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**CAPRICORN MODELS 165/330
DISK STORAGE DRIVE
OPERATION & MAINTENANCE MANUAL**

3314369-01

REV. E, 1/84

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL ENVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE, IN WHICH CASE THE USER AT HIS OWN EXPENSE WILL BE REQUIRED TO TAKE WHATEVER MEASURES MAY BE REQUIRED TO CORRECT THE INTERFERENCE.

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Prepared by
 Technical Publications Dept.

INTRODUCTION

This manual provides maintenance personnel with information necessary to install, operate, and maintain the Capricorn disk storage drive.

The maintenance manual is arranged in five sections and is supported by the Capricorn maintenance diagrams and Logic Term reference appendices. The scope of each section is described by the following paragraphs.

Section I, General Information, contains the Capricorn functions, options, physical and electrical description, and equipment specifications.

Section II, Installation, contains information to enable maintenance personnel to uncrate, inspect, and install the Capricorn in the various applications required (i.e., rack mounting, dual-port option, etc.) Preliminary checks and/or adjustments other than those required for normal maintenance are also contained in this section.

Section III, Operation, explains and shows the location and use of all controls and indicators, as well as procedures for powering up or powering down the disk drive.

Section IV, Theory of Operation, explains the drive operations and gives a detailed description of each function. Simplified logic and block diagrams, timing diagrams, waveforms, and optional descriptions are included.

Section V, Maintenance, contains corrective maintenance procedures.

Appendix A contains reference drawings.

Appendix B contains Logic Term reference aids.

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SECTION I

GENERAL INFORMATION

1.1 GENERAL DESCRIPTION

The Capricorn Model 165/330 disk drives are fixed-media, random-access, rotating memory storage devices that enable the central processing unit (CPU) of a data processing system to store and retrieve blocks (records) of data on rotating disks. The drive functions as the input/output device for the CPU and can operate as a single stand-alone, or it may be operated with similar disk drives in either daisy-chain or radial configurations. The dual-port option allows attachment of the disk drive to two separate controllers.

Capricorn Model 330 disk storage drive has a storage capacity of 330.3 megabytes using sixteen movable heads. Data is stored on a disk stack containing eight recording surfaces (five disks). Capricorn Model 165 disk drive has a storage capacity of 165.9 megabytes utilizing ten heads per cylinder on five recording surfaces (three disks). Capricorn Model 165E, which emulates the Ampex DM9160 SMD drive, uses five heads per cylinder (i.e., ten physical heads on five recording surfaces). Access to data is provided by two moving heads per disk surface. The heads are an integral part of the HDA and never require alignment in the field. Data is recorded on the disk surfaces using modified frequency modulation (MFM) techniques. The standard storage module drive (SMD) read/write interface is the non-return-to-zero (NRZ) type.

For the track-following type servo system the drive incorporates a closed loop. One surface of the disk stack is prerecorded with special servo tracks to provide track-to-track and rotational positioning information. The servo track defines each data track location and contains patterns that generate position information to center the heads precisely over the data tracks during head positioning and read/write operations. Read/write heads are positioned automatically over a special landing zone (located outside the data area) whenever the rotational speed of the disk stack drops below a usable operating level.

The major components of the drive are illustrated in Figure 1-1 and are explained in the following paragraphs.

1.1.1 Diagnostic/Control Panel Assembly

The diagnostic/control panel assembly is mounted on the front of the drive, behind the decorative cover. This panel contains operator controls and indicators and maintenance controls and indicators that enable the user to control the

drive and operate the diagnostics. The operator controls and indicators are accessible whether or not the decorative cover is removed. However, the maintenance controls and indicators are accessible only with the decorative panel opened. A detailed description of each control and indicator is provided in Section III. The diagnostic/control panel assembly also contains a filter that cleans the air entering the drive enclosure.

1.1.2 Chassis Pan Assembly

The chassis pan assembly houses the HDA, drive motor, electronics assembly, power supply, drive cover, and control panel. Optional rails for rack mounting are available.

1.1.3 Head Disk Assembly

A completely sealed head disk assembly (Figure 1-2) envelops the read/write heads, disks, carriage, linear motor, and filters. The spindle-mounted disks are rotated by the drive pulley as the read/write heads fly over the surface of the disk. The linear motor positions the heads over the disk, using positioning information from a dedicated servo surface. Within the sealed module, air that is circulated by the rotation of the spindle is filtered for particles larger than 0.3 microns by one internal filter.

1.1.4 Drive Motor

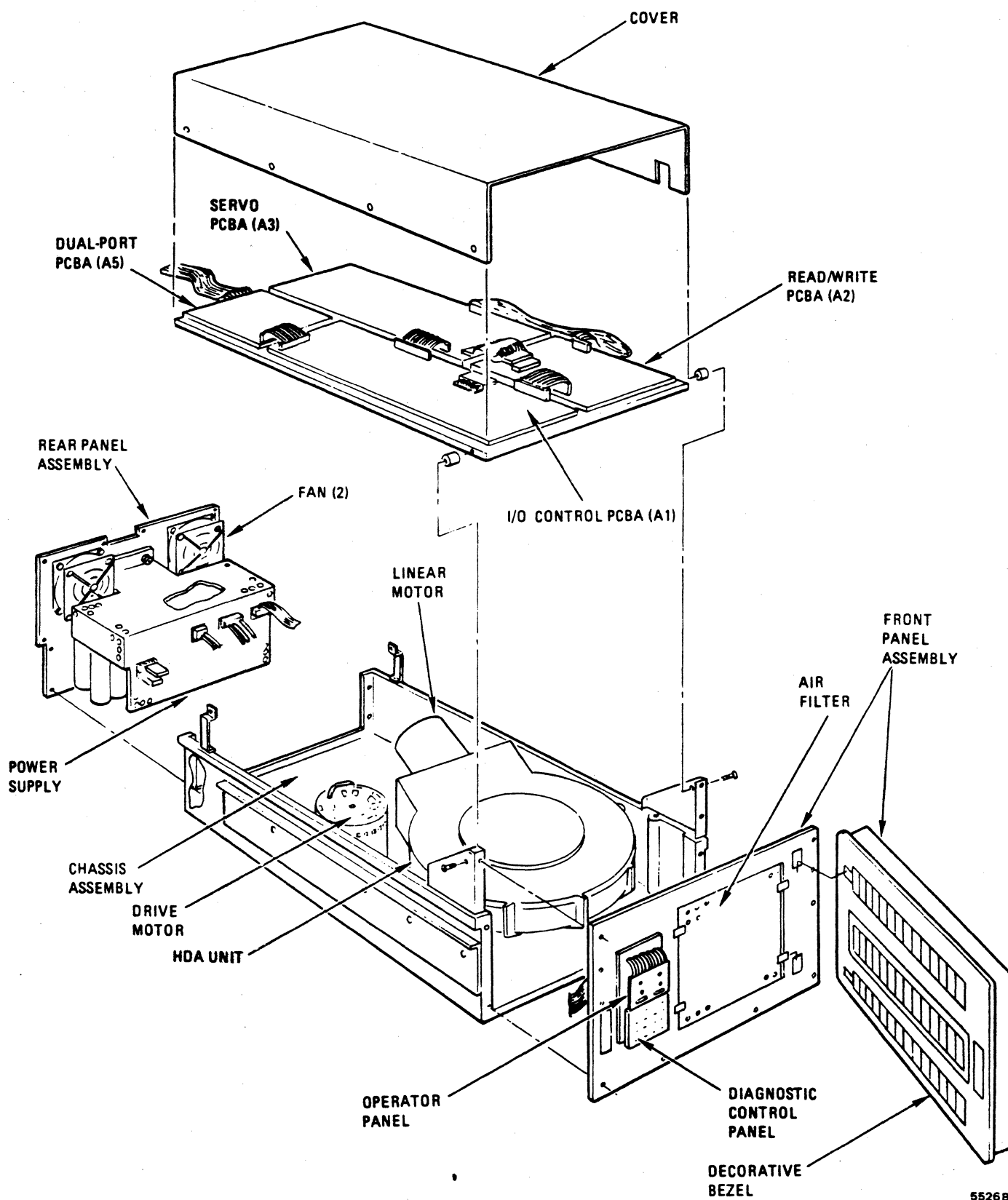
The drive motor is a 1/3-hp induction-type motor that is secured to the chassis with insulated hardware so that ac current from the motor does not circulate in the chassis pan assembly. The drive motor rotates the spindle at 3600 revolutions per minute (RPM).

1.1.5 Electronics Assembly

The electronics assembly, consisting of three standard printed circuit board assemblies (PCBAs) and one optional PCBA, are mounted on an electronic assembly frame that is attached to the chassis pan.

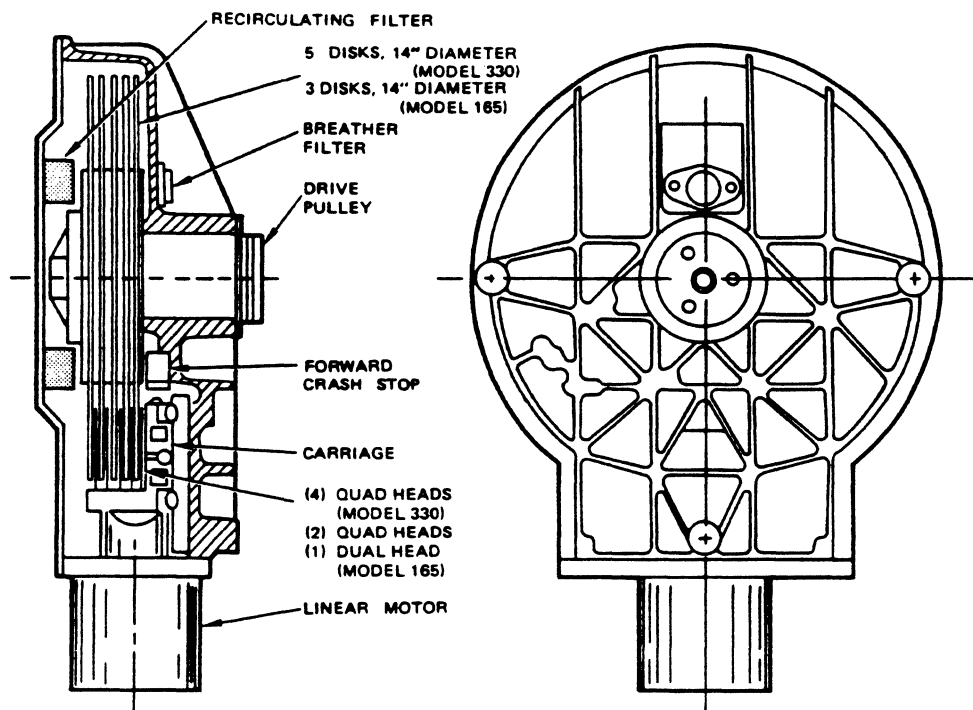
1.1.6 Power Supply

The field-replaceable power supply module, located at the rear of the drive, provides all the dc voltages that are required for drive operations. Two fans, also mounted on the rear panel assembly, exhaust the circulated air from the drive unit.



55268

Figure 1-1. Major Component Location



55138

Figure 1-2. Head Disk Assembly (HDA)

1.2 OPTIONS

Any of the following options or combinations of options are available for the Capricorn disk drive.

1.2.1 Dual Port Option

The dual-port option allows the drive to be accessed through two independent SMD interface ports. With the dual-port option, the drive can be attached to two separate controllers and can be accessed by either controller.

1.2.2 Mounting Options

The standard drive is equipped with rubber mounting feet and may be installed on a table top or appropriate flat surface. With the rack-mount option, drawer slides are provided for mounting the drive in a standard 19-inch rack cabinet.

1.2.3 Power Source Option

The standard drives are configured to operate from 120 vac, 60 Hz, single phase. Drives configured to operate from a

voltage source of 230 vac, 50 Hz, single phase are also available.

1.3 EQUIPMENT CONFIGURATION

The specific configuration of each drive is identified by the equipment identification (ID) nameplate. Identification of the drive configuration is required to determine the applicability of the technical manual.

1.3.1 ID Nameplate

Two labels, ID Nameplate and Field Converted Power Requirements, are located on the external side of the rear panel. The ID Nameplate identifies the equipment by model, part number, issue, applicable power characteristics (i.e., voltage, frequency, start current, and run current), and the unique serial number. (See Figure 1-3A). The Field Converted Power Requirements label is intended for use by the user to record any change made in the field to the power requirements (Figure 1-3B).

AMPEX Computer Products Division El Segundo CA	
CAPRICORN 330	Configuration no. 3316335
Part no. 3313979-11	Serial no.
Voltage 120V ~	Frequency 60 Hz
Start Current: 26 Amp	Run Current: 6 Amp
May be converted to alternative power requirements as indicated on separate power requirements labels.	
Made in U.S.A.	

6135-1

A. Typical Identification Nameplate

POWER REQUIREMENTS			
THIS UNIT HAS BEEN FIELD CONVERTED FOR			
☐ 120V ~	60 Hz	26 Amp Start	6 Amp Run
☐ 120V ~	50 Hz	26 Amp Start	6 Amp Run
☐ 220/240V ~	60 Hz	13 Amp Start	3 Amp Run
☐ 220/240V ~	50 Hz	13 Amp Start	3 Amp Run

6135-2

B. Field Converted Power Requirements

Figure 1-3. Typical Identification Labels

A similar power-requirements (Figure 1-4) label is located on the power supply chassis.

POWER REQUIREMENTS			
THIS UNIT HAS BEEN WIRED FOR			
☐ 120V ~	60 Hz	26 Amp Start	6 Amp Run
☐ 120V ~	50 Hz	26 Amp Start	6 Amp Run
☐ 220/240V ~	60 Hz	13 Amp Start	3 Amp Run
☐ 220/240V ~	50 Hz	13 Amp Start	3 Amp Run

6135-3

Figure 1-4. Typical Power Requirements Label

1.3.2 Technical Manual Applicability

Factory or field changes in the equipment are reflected in the technical manual by means of change notices. Change notices contain the technical manual publication number, the change number, and the changes that are to be incorporated into the manual.

1.3.2.1 Tentative Change Notice

A tentative change notice reflects changes associated with critically important equipment modifications. A tentative change notice instructs the user how to mark up the technical manual so that it reflects the equipment configuration as it appears immediately after the completion of the retrofit.

1.3.2.2 Permanent Change Notice

A permanent change notice updates the technical manual by reflecting engineering changes. It also replaces previously issued tentative change notices. Obsolete pages from the technical manual are removed and replaced by permanent change pages.

1.4 FUNCTIONAL CONCEPT

The simplified block diagram in Figure 1-5 shows the functional concept of the Capricorn disk drive. Additional detailed explanations of the logic areas occur in Section III.

1.4.1 Interface

The interface logic translates the input/output signals of the disk drive to ensure drive-to-controller signal compatibility. The dual-port interface permits the drive to communicate with two control units through two identical interfaces designated Port A and Port B. Disk drive logic signal levels are transistor-to-transistor logic (TTL) compatible. The transmission line signals are differential signals.

1.4.2 Bus Arbitration and Select Logic

With the dual-port option, the drive is connected to two separate controllers. However, the drive can communicate with only one of the two controllers at a time. The bus arbitration and select logic determines which controller has priority for a read/write operation.

1.4.3 Read/Write Logic

To execute read or write commands, the drive must be free of faults and the selected head must be at the correct location on the disk (i.e., on cylinder). During a read command, the read/write logic recovers data from the disk, processes the data, and transfers the data to the controller. During a write command, the read/write logic receives data from the controller, processes the data and writes it on the disk.

1.4.4 Head Select Logic

The head select logic receives, decodes, and stores the address of a specific head. The select logic also compares the logical input selection with the logical unit number preset in the unit identification microswitch.

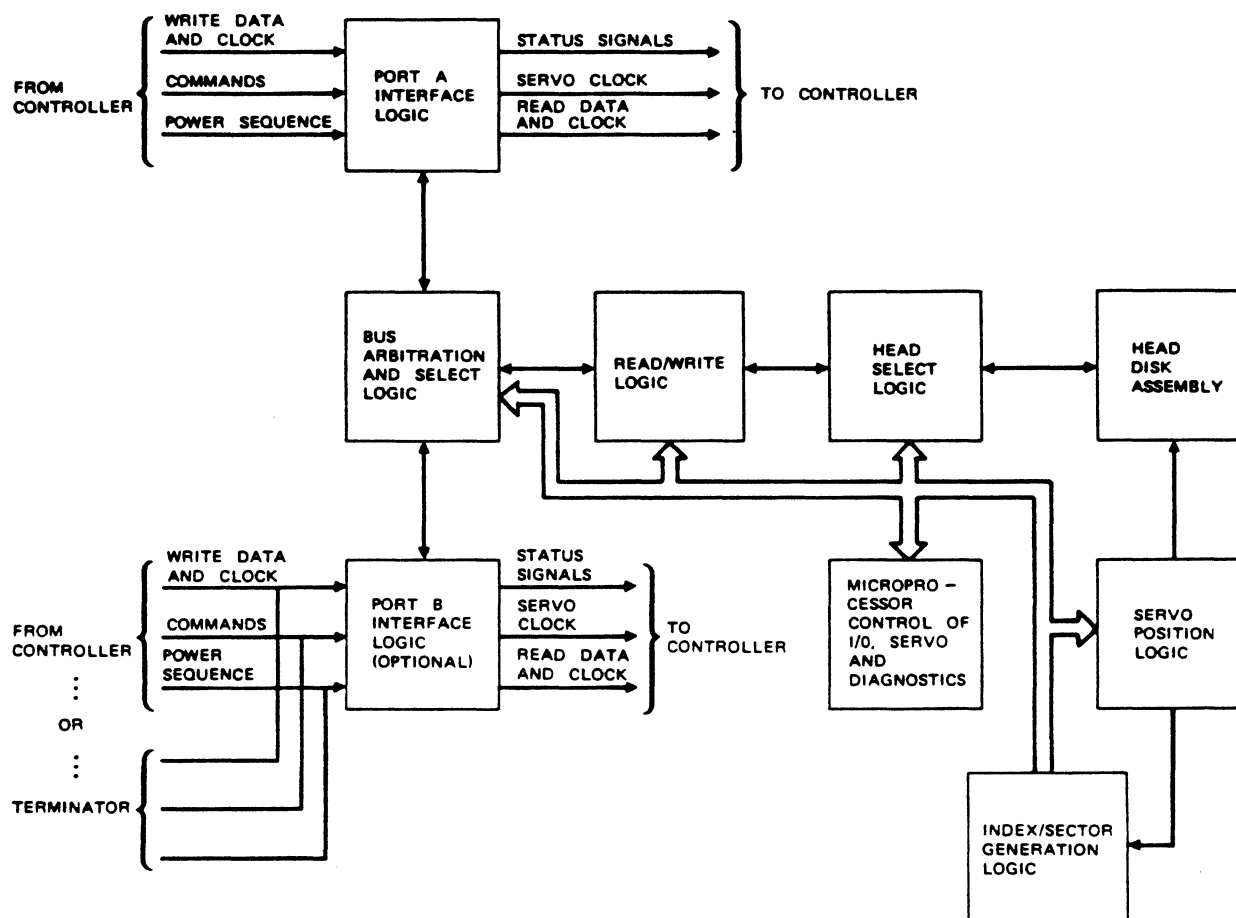


Figure 1-5. Capricorn Simplified Block Diagram

5514 A

1.4.5 Servo Position Logic

The servo position logic converts analog information from the servo head to a dc position signal. This position signal provides location feedback to keep the head position locked to the cylinder. The servo position logic also provides analog-to-digital conversion of the servo signal to allow sensing of the rotational position of the disk stack. The servo clock signal generated by the servo position logic is used for synchronizing the frequency of write data to the disk drive.

1.4.6 Index/Sector Generation Logic

Rotational position information is obtained from the pre-recorded servo surface of the disk stack through the servo

position electronics. Clock gaps exist on each servo track to indicate the reference point (index) for each track. The index detector logic senses the presence of these gaps to determine the index point. Each track may be divided into a sector by counting the servo pulses recorded on the servo track. The sector counter is programmable to provide 4 through 128 sectors per track.

1.5 EQUIPMENT SPECIFICATIONS

Performance characteristics for drives are listed in Table 1-1. Environmental specifications are listed in Table 1-2. Power requirements are listed in Table 1-3 and shown in Figure 1-6.

Table 1-1. Performance Characteristics

Characteristics	Specifications
SPINDLE	<u>MODEL 330</u> <u>MODEL 165</u> <u>MODEL 165E</u>
Rotational Speed	3600 (+2.5%, -3.5%) rpm
Latency Time (Defined as the time required for read/write heads to reach a particular sector or data record on a given track after completion of a seek command or initial selection.)	
Average	8.33 milliseconds
Maximum	17.3 milliseconds
Start-Up Time (The time that elapsed from initiating the power-up sequence until read/write heads are positioned at track zero and drive is ready to seek, read, or write.)	15 seconds (maximum)
Stop Time (The time required for stack to come to a complete stop after removal of power.)	15 seconds (maximum)
HEAD POSITIONING ACCESS TIME	
(Access time is defined as the time required to position the read/write heads from a seek initialization until the drive becomes ready.)	
Track-to-Track	6 milliseconds
1024 Cylinders (maximum seek)	55 milliseconds
823 Cylinders (maximum seek)	50 milliseconds (maximum)
Average (Average seek time equals the sum of the times to do all possible seeks divided by the total number of seeks possible.)	30 milliseconds
ERROR RATES *	
Position errors	1 in 10^6 seeks
Recoverable read errors	1 in 10^{10} bits
Unrecoverable read errors	1 in 10^{12} bits
MEDIA DEFECTS (MAXIMUM NUMBER)	
Defects per drive (Model 330)	400 max
Defective tracks per drive (Model 330)	40 max
Defects per drive (Model 165)	250 max
Defective tracks per drive (Model 165)	25 max

* These error rates are valid only when the drive is being used according to specifications. Media defects or equipment failures are excluded. Written data should be verified as being correctly written. All media defects should be flagged.

Table 1-1. Performance Characteristics (Cont.)

Characteristics	Specifications		
STORAGE CHARACTERISTICS	MODEL 330	MODEL 165	MODEL 165E
Number of Disks	5	3	3
Data Surfaces	8	5	5
Capacity (Megabytes)	330.3	165.9	165.9
Bytes/Cylinder	322,560	201,600	100,800
Bytes/Track	20,160	20,160	20,160
Cylinders**	1024	823	1645
Tracks/Cylinder	16	10	5 (logical)
Tracks/Surface	2048	1646	1645
Servo Heads	1	1	1
Read/Write Head Width	0.0007"	0.0007"	0.0007"
Track Spacing (960 TPI) center to center	0.001"	0.001"	0.001"
Bit Density (Inner Track)	6250 bpi	5950 bpi	5950 bpi
Disk Diameter	14"	14"	14"
Recording Technique	MFM	MFM	MFM
Disk Coating Material	Coated oriented magnetic oxide	Coated oriented magnetic oxide	Coated oriented magnetic oxide
Data Transfer Rate (MFM encoding)	1,209,600 – 8-bit bytes/ sec. nom. (9,676,800 bits/sec. nom.)	1,209,600 – 8-bit bytes/ sec. nom. (9,676,800 bits/sec. nom.)	1,209,600 – 8-bit bytes/ sec. nom. (9,676,800 bits/sec. nom.)

** Ten additional cylinders are reserved for diagnostic maintenance and are not available to the user.

Table 1-2. Capricorn Environmental Requirements

Condition	Storage	Transit	Operating
TEMPERATURE	+40°F to 140°F —40°C to 60°C	—40°F to 140°F —40°C to 60°C	50°F to 110°F 10°C to 43.3°C
TEMPERATURE GRADIENT (Per Hour)	27°F 15°C	27°F 15°C	18°F 10°C
RELATIVE HUMIDITY (NO CONDENSATION)	10% to 90%	10% to 90%	20% to 80%
HUMIDITY GRADIENT	10% per hr.	10% per hr.	10% per hr.
ALTITUDE (IN FEET)	—980 to 40,000	—980 to 40,000	—980 to 10,000
VIBRATION (VERTICAL)	5—50 Hz 0.01 in. disp. 50—500 Hz 2 gs acc.	5—50 Hz 0.01 in. disp. 50—500 Hz 2 gs acc.	5—10 Hz 0.004 in. disp. 10—15 Hz 0.02 gs acc. 15—50 Hz 0.0016 in. disp. 50—500 Hz 0.20 gs acc.

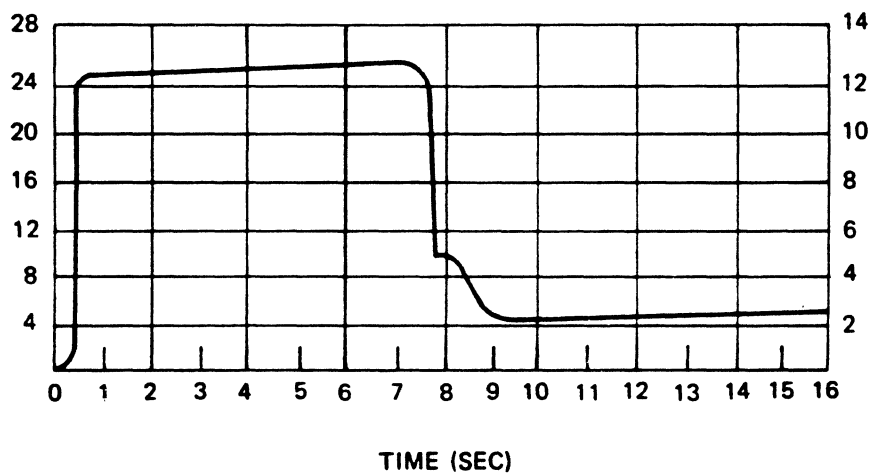
INTERMITTENT SHOCK (VERTICAL) Up to 2.0 gs not exceeding 10 msec in duration. Time between consecutive shocks will not be less than 0.5 seconds.

Table 1-3. Power Requirements

Item	60 Hz	50 Hz
Voltage (Single Phase)	120+12%, -17%	230+12%, -17%
Frequency	60±1.0 Hz	50±1.0 Hz
Start Current (10 seconds)	26 Amps	14 Amps
Run Current	6 Amps	4 Amps
Line Current Versus Start-Up Time	-----See Figure 1-6 -----	

120V AMPS

230V AMPS



6022

MAXIMUM START-UP CURRENT (120V 60 Hz/230V 50 Hz) CAPRICORN DRIVE**Figure 1-6. Line Current Versus Startup**

SECTION II

INSTALLATION

2.1 GENERAL

This section contains unpacking, installation, and checkout information for the Capricorn Model 165/330 disk drive.

2.2 UNPACKING

Prior to unpacking the drive, perform a visual inspection of the packaged drive to ascertain whether or not any damage has occurred during shipment.

1. Verify by means of shipping documents all items have been received.
2. Open protective shipping carton at top.
3. Remove drive from shipping carton.
4. Remove plastic cover.
5. Visually inspect each packaged article to determine whether or not damage has occurred during shipment.
6. Verify connectors, front panel controls and indicators, and protruding parts are undamaged.
7. Check ID nameplate against shipping papers to assure correctness of drive part number and serial number (reference paragraph 1.3.1).
8. Inventory following optional loose items:
 - Control Cable (one per drive).
 - Read/Write cable (one per drive).
 - AC power cable (one per drive).
 - Drive terminator plug (one per string of single-port drives and two per string of dual-port drives).
 - Rack mount slides.
9. When practical, store shipping containers for reuse.
10. Record damage and report damage to the applicable carrier.

2.3 EQUIPMENT PLACEMENT

Equipment placement consists of mounting the drive and planning the layout, routing the input/output cables, and grounding the equipment.

2.3.1 Equipment Mounting

The standard drive is designed for desk- or table-top placement. The optional rack-mount provides hardware for mounting the drive in a standard 19-inch rack.

2.3.1.1 Standard Table-Top Drive Mount

The standard Capricorn disk drive is equipped with mounting pads (Figure 2-1) to permit positioning the drive on a flat level surface (e.g., a table top, bench top, etc.). The dimensions of the standard table-top drives are shown in Figure 2-2.

2.3.1.2 Option Rack Mount

With the rack-mount option, the drive can be slide-mounted into a standard 19-inch rack. Cabinet spacing requirements for either single-drive or multi-drive installation are shown in Figure 2-3. The slide kit comprise the parts listed in Figure 2-4. The following steps explain the procedure for installing the Capricorn in a standard rack.

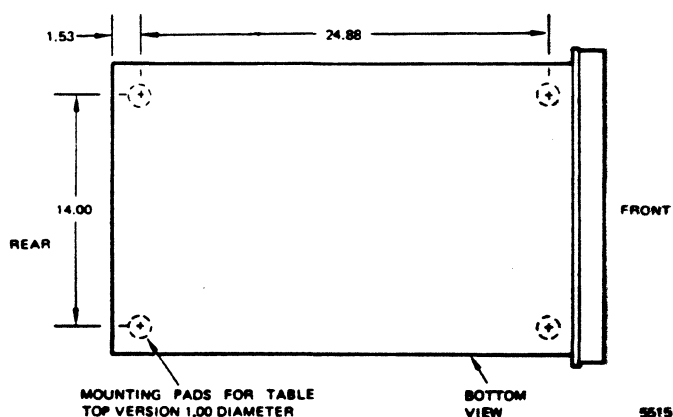


Figure 2-1. Location of Mounting Pads

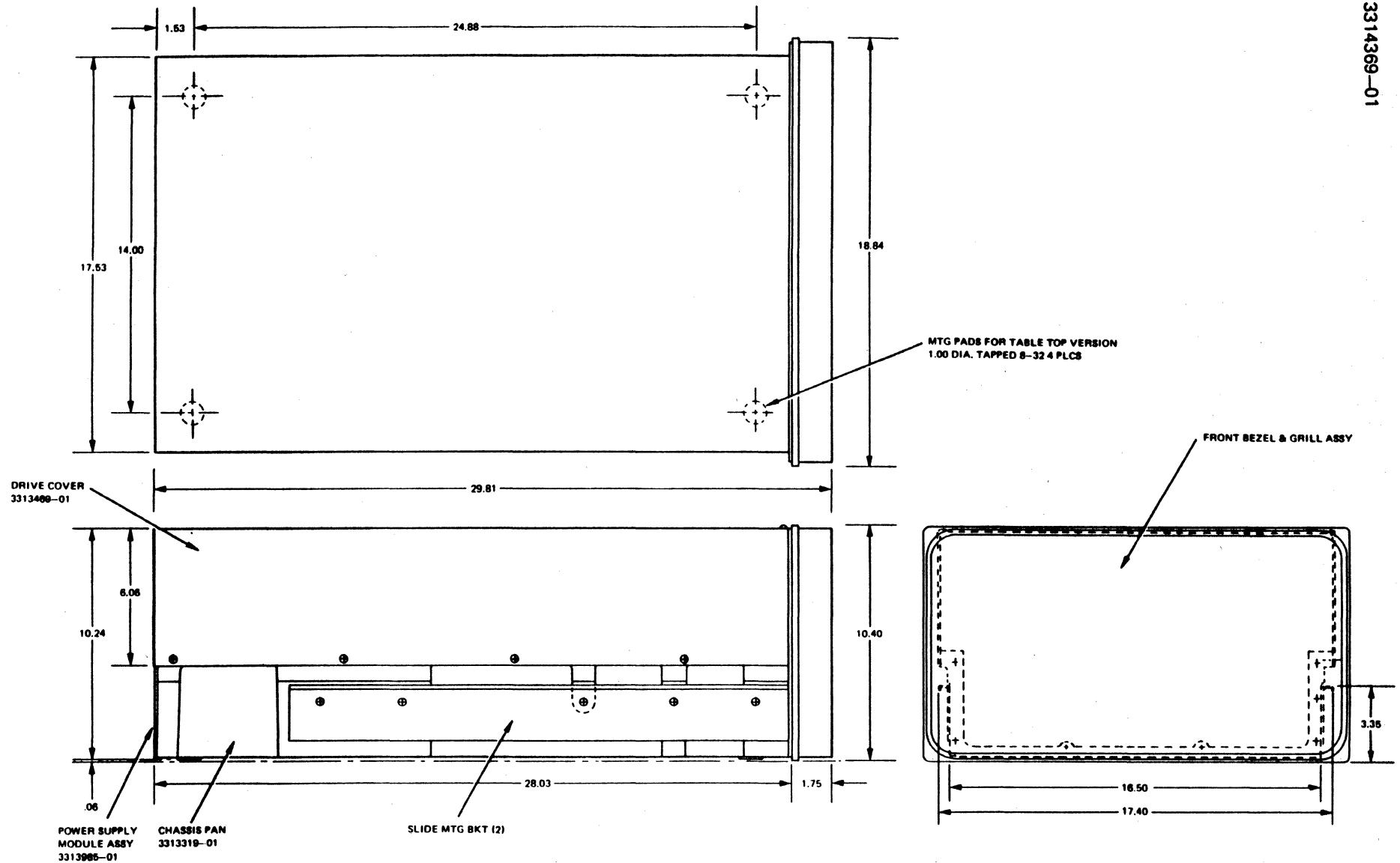


Figure 2-2. Capricorn Space Requirements

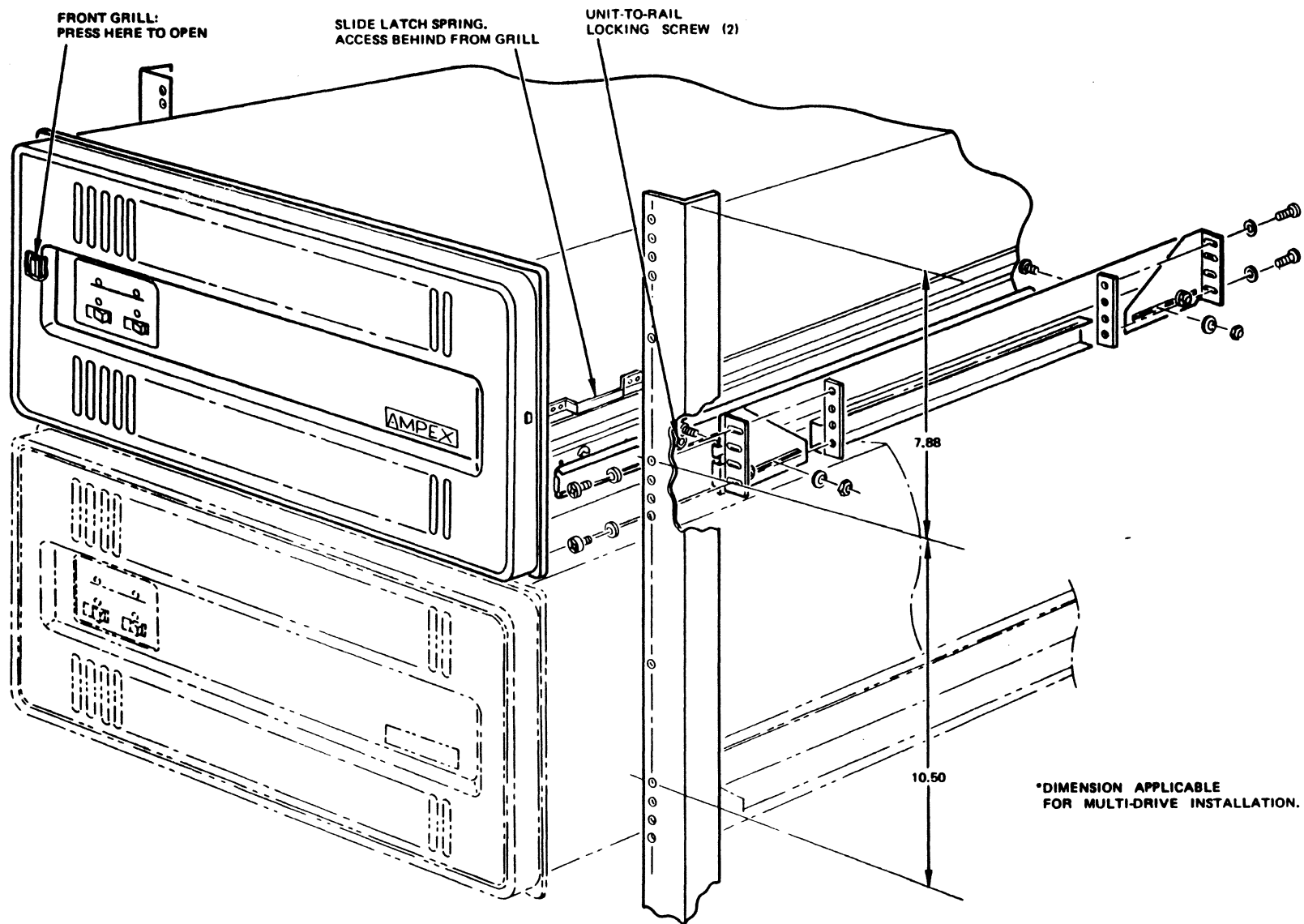
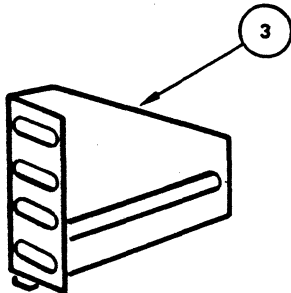


Figure 2-3. Slide Mount Installation Details

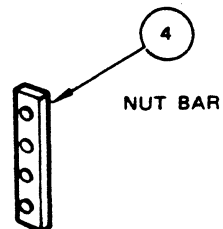
8816A

SLIDE KIT PARTS LIST

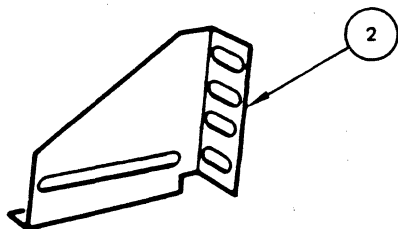
ITEM	AMPEX PART NO.	DESCRIPTION	QTY
1	530-495	SLIDE, BALL BEARING	1 PAIR
2	530-496	MOUNTING BRACKET, LEFT-FRONT/RIGHT-REAR	2
3	530-497	MOUNTING BRACKET, RIGHT-FRONT/LEFT-REAR	2
4	530-498	BAR, NUT	4
5	471-098	SCREW, PANHEAD, 10-32X 0.500 LG	8
6	471-567	SCREW, BINDERHEAD, 8-32X 0.375 LG	10
7	501-010	WASHER, FLAT NO. 8	8
8	501-070	WASHER, FLAT NO. 10	8
9	496-006	NUT, HEX, WITH ASSEMBLY WASHER NO. 8	8



FRONT MOUNTING BRACKET ON RIGHT SIDE
REAR MOUNTING AND BRACKET ON LEFT SIDE



NUT BAR



FRONT MOUNTING BRACKET ON LEFT SIDE
REAR MOUNTING BRACKET ON RIGHT SIDE

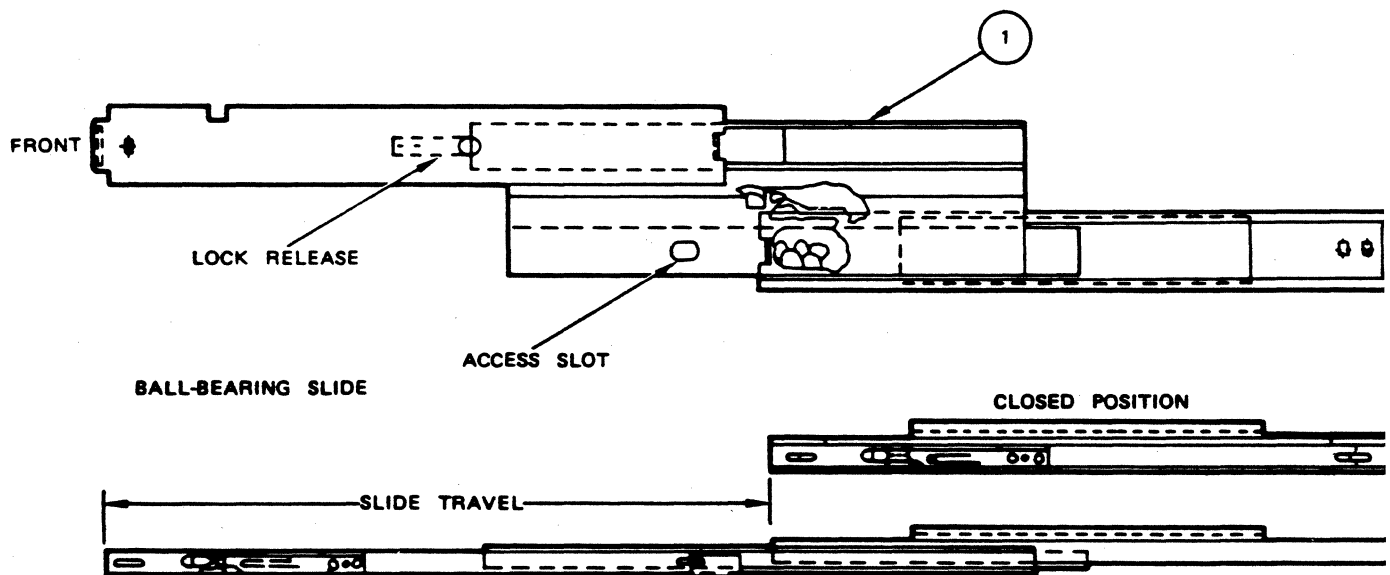


Figure 2-4. Slide-Kit Parts

CAUTION

The drive weighs about 128 pounds. When it is moved forward for maintenance, the center of gravity is also moved forward; therefore, unless the rack is counter balanced the entire rack could fall forward.

NOTE

Do not tighten the bracket screws during the following two steps.

1. Attach front and rear mounting brackets to right slide rail using attaching hardware as shown in Figure 2-5.

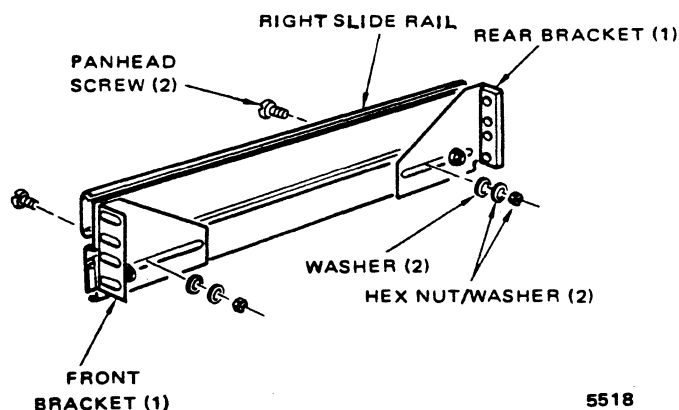


Figure 2-5. Mounting Bracket Installation

2. Attach front and rear mounting brackets to left slide rail using attaching hardware as described in step 1.

NOTE

Both front and rear brackets can be adjusted to fit during installation of the slide rails.

3. Align right slide rail to cabinet mounting holes as shown in Figure 2-6; attach front and rear mounting brackets to respective nut bars using attaching hardware as shown in Figure 2-6, and tighten binder head screws.
4. Attach left slide rail to cabinet in the same manner as step 3, and tighten binderhead screws.

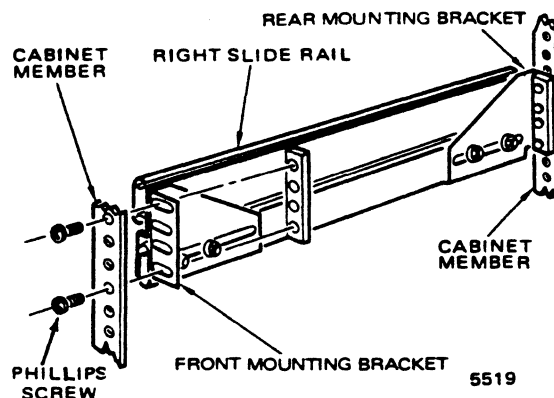


Figure 2-6. Slide Rail Assembly Installation

5. Tighten all panhead screws on mounting brackets.
6. Depress lock release (Figure 2-4) and extend slide rail to full length of slide travel where slides lock to extended position.
7. Place drive onto extended slide rail as shown in Figure 2-7.
8. Install unit-to-rail locking screw (Figure 2-4, Item 6 in slide Kit Parts List) to fasten top member of slide to drive unit as shown in Figure 2-3.
9. Release spring lock on each side and push drive unit into drawer to closed position.
10. Check latch spring (inside front grill); adjust spring as required.

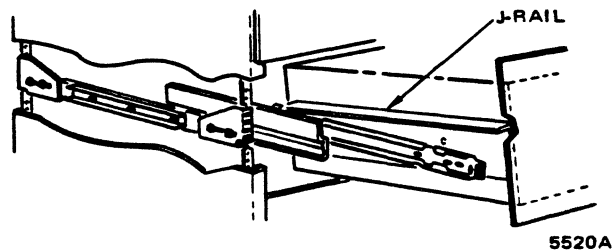


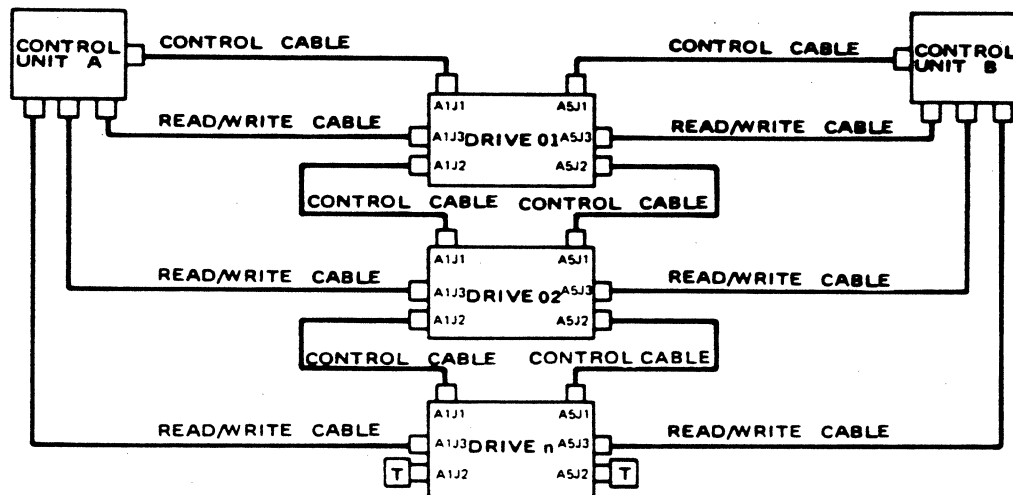
Figure 2-7. Placement of Unit on Slide Rails

2.3.2 Daisy-Chain and Radial Configurations

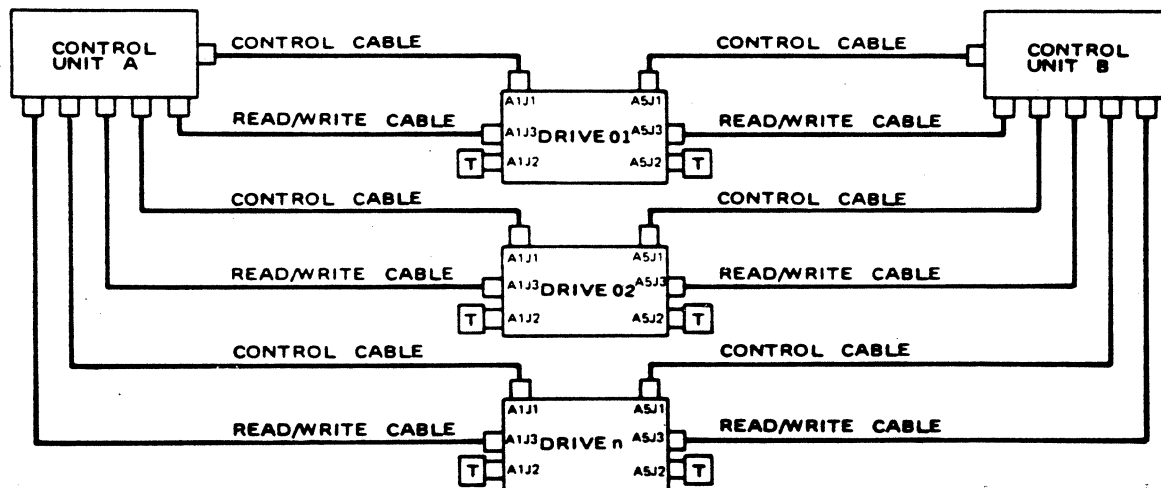
Both the standard and dual-port versions of the drive provide the capability up to 16 drives in either the daisy-chain or radial configuration. Both configurations for the dual-port versions are shown in Figure 2-8. Configurations shown in Figure 2-8 are also applicable to the standard single-port versions except that connectors A5J1, A5J2, and A5J3 of the drive are not used.

In the daisy-chain configuration, the control cable connects the controller to the first unit. Other control cables connect drive to drive, and the last drive in the string has a terminator installed on it (Figure 2-8, View A). Individual read/write cables connect each drive directly to the controller.

In the radial configuration, individual control and read/write cables connect each drive directly to the controller, and each drive has a terminator installed on it (Figure 2-8, View B).



VIEW A, DAISY-CHAIN CONFIGURATION



VIEW B, RADIAL CONFIGURATION

- NOTES:
1. CONTROL CABLE, P/N 3308179-XX, MAXIMUM CUMULATIVE LENGTH-100 FEET.
 2. READ/WRITE CABLE, P/N 3308186-XX, MAXIMUM LENGTH-50 FEET.
 3. **T** = TERMINATOR, P/N 3309833-01.
 4. DC GROUND CABLE TO BE CUSTOMER SUPPLIED, JACKETED, FLAT BRAID TERMINATED WITH A RING TONGUE TO FIT OVER THE 10/32 SCREW ON THE DRIVE IS RECOMMENDED.

Figure 2-8. System Cabling Configuration

5521B

2.3.3 Grounding

An ac power cable is provided with each drive. In all installations the green wire (120 vac, 60 Hz) or green/yellow wire (230 vac, 50 Hz) must be connected to the ac main safety ground. Connector AC GND is located on the power supply panel. The safety ground connects to the frame and to all major electrical components such as motors and fans. To meet UL, CSA, and VDE approval, each drive is shipped with this ac safety ground and the dc ground tied together at one point within the drive (Figure 2-9). This ac-to-dc jumper should be removed when the drive is installed.

Each drive must be connected to the system ground grid or single-point ground with a low RF impedance ground strap of 1/2-inch (minimum) insulated flat braid. The ground strap should be connected to the dc ground post of the respective drive (Figure 2-9), routed with the read/write I/O cable (i.e., B-cable or Star cable) to the disk controller; and thence routed with the controller ground to the system ground point.

Shield I/O cables must be used in systems where the cables are not protected from radiated RF noise or where the cables are a source of RF noise that interferes with other equipment. If shielded cables are required, the shields must be tied together through the daisy chain and connected to the dc grounds with the RF ground straps only at the ends of the daisy chain.

For dual-port installations, all drives should be grounded via only one of the two systems controllers to a common system grounding point.

NOTE

The ground strap should be cleaned before installation to insure good ground connection.

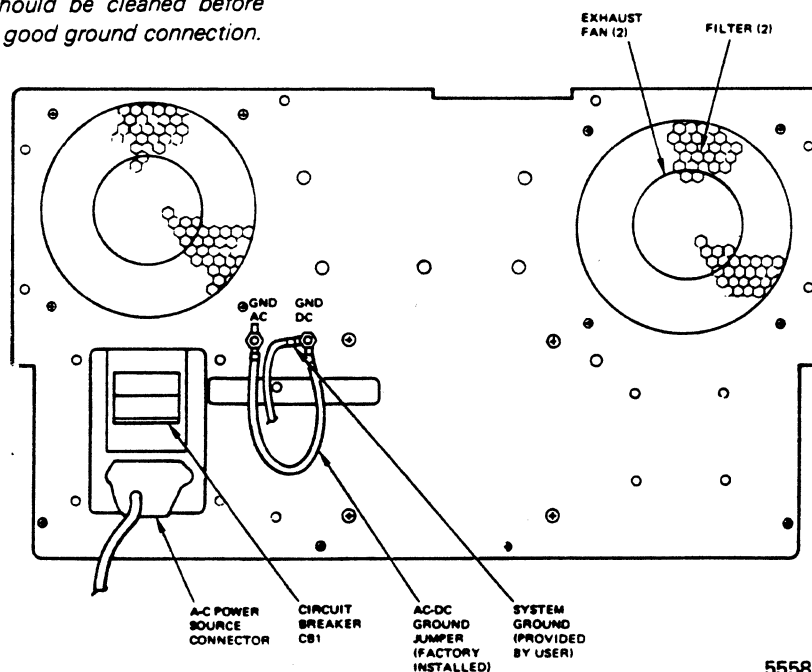


Figure 2-9. Power Supply Rear View

2.4 PREINSTALLATION CHECKS

The following procedure is a step-by-step set of instructions for checking the drive servo, read/write, and safety circuits for proper operation. These steps are to be performed on a new drive prior to system installation, or may be used as a preliminary start for isolating trouble on a defective drive.

1. Remove top cover in accordance with paragraph 5.4.2.
2. Inspect interior of drive for loose or broken parts and tighten all loose screws and hardware.
3. Verify interconnectors between PCB assemblies are secure.
4. On input/output microprocessor control PCBA (A1), hereafter referred to as I/O control PCBA (A1), set sectors-per-track switches (Figure 3-2) to correct number of sectors as described in paragraph 3.2.2.1.
5. On I/O control PCBA (A1), set Drive Select switch to assigned unit address (paragraph 3.2.2.2.)
6. On I/O control PCBA (A1), set LOCAL/REMOTE switch to LOCAL (paragraph 3.2.2.3).
7. On diagnostic control panel (A4), set DIAG/NORMAL switch to DIAG position (paragraph 3.2.1).

8. Connect applicable power cable (Figure 2-10) between drive and ac power source, and apply power to drive.
9. Ascertain both exhaust fans are running.
10. Run diagnostic tests in accordance with paragraph 5.2 to verify correct drive performance.
11. Remove power to drive.
12. On I/O control PCBA (A1), set REMOTE/LOCAL switch to REMOTE position.
13. On diagnostic panel (A4), set DIAG/NORMAL switch to NORMAL.
14. Replace top cover in accordance with paragraph 5.4.2.

NOTE

The drive is now ready to be connected to the using system.

2.5 SYSTEM INSTALLATION

Installation of the drive consists of connecting the power and input/output cables, setting the I/O control PCBA switches, setting the dual-port option PCBA switches and performing initial startup. System grounding must conform to the requirements of paragraph 2.3.3.

2.5.1 Connector and Cable Requirements

Cable connector requirements are listed in Table 2-1. The connectors for the flat ribbon-type input/output cables are located on the I/O control PCBA and on the optional dual-port PCBA as shown in Figure 2-11 and listed in Table 2-2. Power cords supplied with 50- and 60-Hz drives are shown in Figure 2-10.

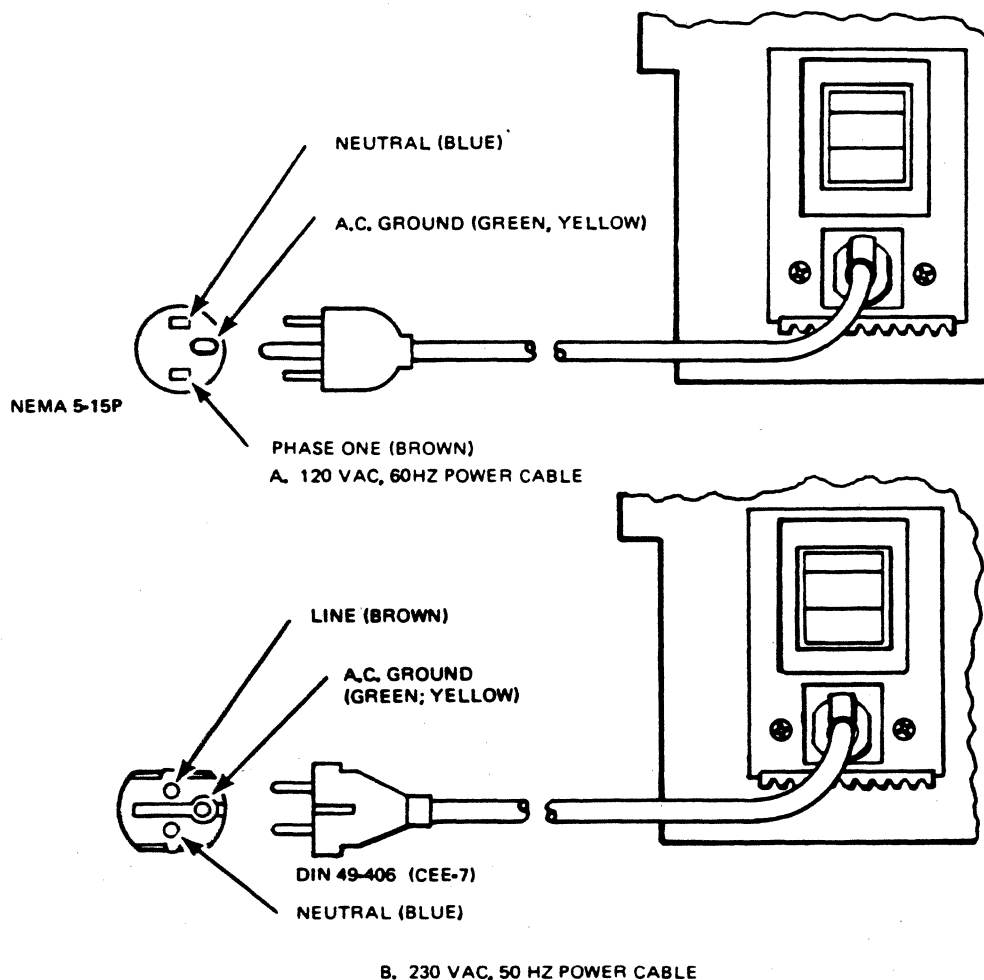
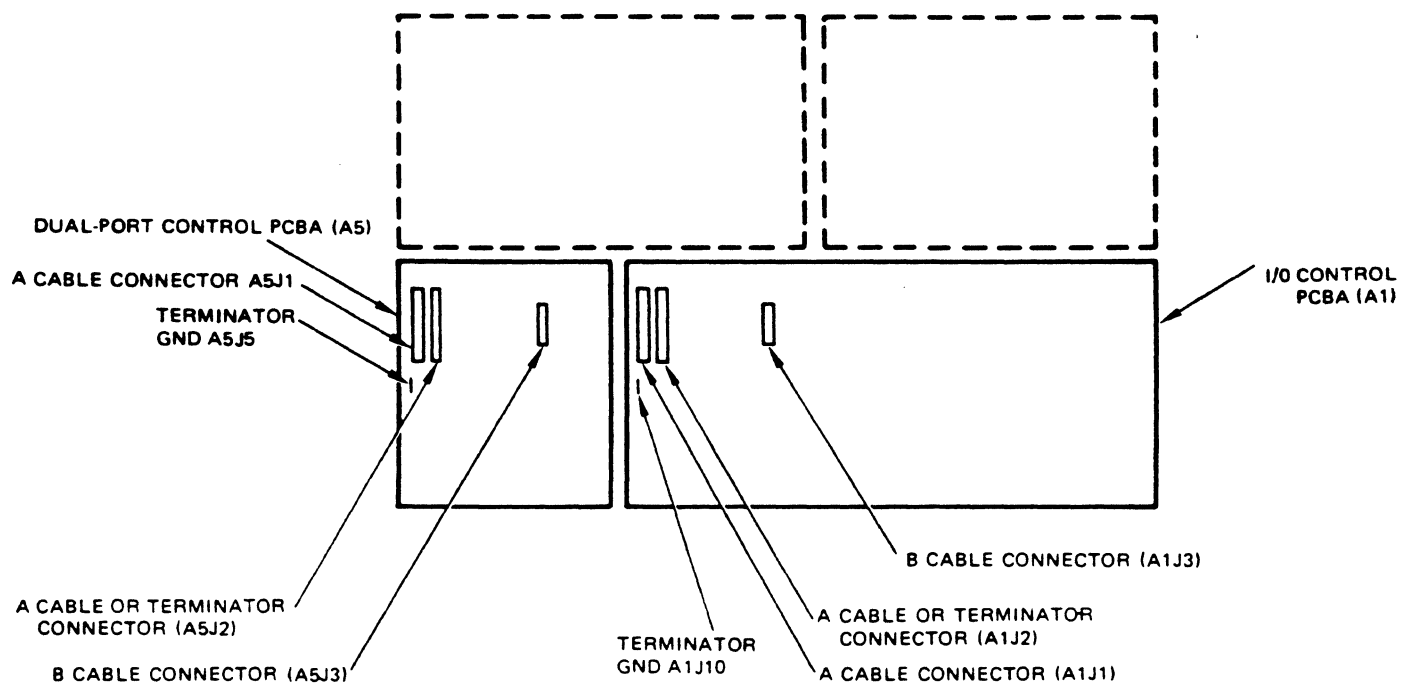
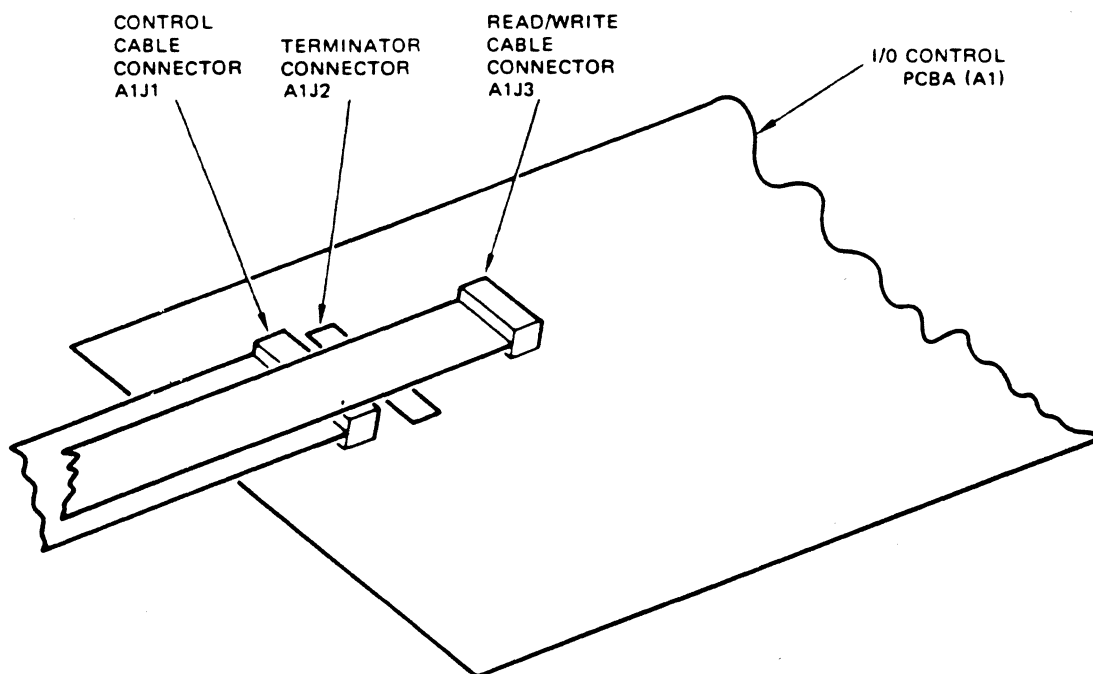


Figure 2-10. Power Cable



A. LOCATION OF I/O CONNECTORS



5522C

B. SINGLE-DRIVE SYSTEM I/O CONNECTIONS

Figure 2-11. I/O Cable Attachment

Table 2-1. Cable Connector Data

Cable Connector	Description
Control Cable (3308179) Cable connector (used on both ends of cable) Mating drive or control unit connector	60-position, Ampex P/N 88012-2 or Ansley P/N 609-6001M Pin header, 60-pin, straight contact, Amp P/N 3-87422-0 Pin header, 60-pin, right-angle contact, Amp P/N 87365-7
Read/Write cable (3308186) Cable connector (used on both ends of cable) Mating drive or control unit	26-position, Ampex P/N 86905-2 or 3M P/N 3399-3000 or Ansley P/N 609-2601M Pin header, 26-pin, straight contact, Amp P/N 1-87422-5 Pin header, 26-pin, right-angle contact, Amp P/N 87365-3
Ac Power Connector 60 Hz, 120 Vac operation (Figure 2-10A) 50 Hz, 230 Vac operation (Figure 2-10B)	120 V, 15 amp, 60 Hz, 1-phase, 2-pole, 3-wire male connector configuration: NEMA 5-15P 230 V, 10 amp, 50 Hz, 1-phase, 2-pole, 3-wire male connector configuration: DIN 49-406 (CEE-7)

Table 2-2. System Cables and Related Connectors

Name	From	To	Part Number
Control Cable	Control Unit A Control Unit B A1J2* A5J2**	A1J1 A5J1 A1J1 on next drive A5J1 on next drive	3308179-XX
Read/Write Cable	Control Unit A Control Unit B	A1J3 A5J3	3308186-XX
Power Cable	Ac Power Source	Power Control Panel	084-078- 50 Hz 084-079- 60 Hz

* Control terminators P/N 3309833-01, must be installed in I/O connectors A1J2 if the drive is the only unit or is the last unit in a daisy-chain string, or is in the radial configuration.

** On a dual-port configuration, control terminators P/N 3309833-01, must be installed in I/O connectors A1J2 and A5J2 if the drive is the only unit or is the last unit in a daisy-chain string or is in the radial configuration.

2.5.1.1 Control Cable

The ribbon-type control cable carries control and status information between the drive and the controller. Two control cables (one for each port) are required for each dual-port drive. The cables connect the drive either to the two control units or, in a daisy-chain configuration, to the previous dual-

port drive. Refer to Table 2-2 and Figure 2-11 for connector information. If the drive is the last unit in a daisy-chain string, control terminators, P/N 3309833-01, must be installed in I/O connectors A1J2 (Port A) and A5J2 (Port B). Maximum cumulative length of the ribbon-type control cannot exceed 100 feet. Pin assignments and signal polarities are listed in Table 2-3.

Table 2-3. Control I/O Pin Assignments

Signal Name	Pin Polarity (Active)		Source
	-	+	
Unit Select 2 (0)	23	53	Control Unit
Unit Select 2 (1)	24	54	Control Unit
Unit Select 2 (2)	26	56	Control Unit
Unit Select 2 (3)	27	57	Control Unit
Select Enable (Unit Select Tag)	22	52	Control Unit
Set Cylinder (Tag 1)	1	31	Control Unit
Set Head Address (Tag 2)	2	32	Control Unit
Control Select (Tag 3)	3	33	Control Unit
Bus Out 0	4	34	Control Unit
Bus Out 1	5	35	Control Unit
Bus Out 2	6	36	Control Unit
Bus Out 3	7	37	Control Unit
Bus Out 4	8	38	Control Unit
Bus Out 5	9	39	Control Unit
Bus Out 6	10	40	Control Unit
Bus Out 7	11	41	Control Unit
Bus Out 8	12	42	Control Unit
Bus Out 9	13	43	Control Unit
Device Enable (Open Cable Detector)	14	44	Control Unit
Index	18	48	Drive
Sector Mark	25	55	Drive
Fault (R/W Unsafe)	15	45	Drive
Seek Error	16	46	Drive
On Cylinder	17	47	Drive
Unit Ready	19	49	Drive
Write Protected	28	58	Drive
Address Mark	20	50	Drive
Busy	21	51	Drive
Power Sequence Pick	29		Control Unit
Power Sequence Hold	59		Control Unit
Bus Out 10 (DM9160)	30	60	Control Unit

Y

2.5.1.2 Read/Write Cable

The ribbon-type read/write cable transfers all NRZ data and clock signals between the control unit and the drive. Refer to Table 2-2 and Figure 2-11 for connector information.

Read/Write cables (one for each port) are required for each dual-port drive. Maximum length of the read/write cable is 50 feet. Pin assignments and signal polarities are listed in Table 2-4.

Table 2-4. Read/Write I/O Pin Assignments

Signal	Pin Polarity (Active)		Ground	Source
	—	+		
Ground			1	
Servo Clock	2	14		Drive
Ground			15	
Read Data	3	16		Drive
Ground			4	
Read Clock	5	17		Drive
Ground			18	
Write Clock	6	19		CU
Ground			7	
Write Data	8	20		CU
Ground			21	
Unit Selected	22	9		Drive
Seek End	10	23		Drive
Ground			11	
Reserved for Index	12	24		Drive
Ground			25	
Reserved for Sector	13	26		Drive

2.5.1.3 Terminator

If the drive is the last drive in a daisy-chain installation, or is the only drive unit connected to the controller, terminators (P/N 3309833-01) must be installed in I/O connectors A1J2 and A5J2. If another drive is to be added to the string, remove the terminators, connect control cable from A1J2 and A5J2 to A1J1 and A5J1, respectively, on the new drive, and install the terminators in A1J2 and A5J2 of that drive. **BE SURE THE LAST DRIVE IN THE STRING HAS TERMINATORS INSTALLED.**

All control signal lines are terminated with 56-ohm resistors from each side of the balanced differential line to ground at both the transmitting and receiving ends. At the drive end of the cable, the terminator resistors are located in the aforementioned terminator plug attached to the control cable output connector of the last drive in the string.

The Read Data, Write Data, Servo Clock, Read Clock, and Write Clock lines are terminated with 68-ohm resistors from each side of the differential line to ground at the receiving end only. Other control and status lines in the read-write cable are terminated at both ends of the cable with 56-ohm resistors from each side of the differential lines to ground.

2.5.2 Input Power Consideration

The standard power source for the drive is 120 volt, single-phase, 60 Hz power. The drive can also be configured to accommodate 230 volt, single-phase, 50 Hz power. Drives shipped from the factory are wired for the power source specified at the time of order. Before performing the drive installation, if any question exists as to whether the drive matches the source power, the actual available line voltage must be measured and the drive power components verified as described in paragraph 2.5.2.1 or 2.5.2.2, as applicable.

2.5.2.1 Power Verification for 60 Hz Configuration

1. Verify ID Nameplate (paragraph 1.3.1) indicated 120 volt, 60 Hz power.
2. Verify drive motor is stamped 60 Hz.
3. Verify drive motor pulley is stamped 60 Hz.
4. Verify drive motor belt is identified as 3313379-01.
5. Verify power supply is identified as 3313985-01.

6. Verify transformer is stamped 60 Hz.
7. Verify circuit breaker CB1 (Figure 2-9) is stamped 15A.

2.5.2.2 Power Verification for 50 Hz Configuration

1. Verify ID Nameplate (paragraph 1.3.1) indicates 230 volt, 50 Hz power.
2. Verify drive motor is stamped 50 Hz.
3. Verify drive motor pulley is stamped 50 Hz.
4. Verify drive motor belt is identified as 3313379-02.
5. Verify power supply is identified as 3313985-02.
6. Verify transformer is stamped 50 Hz.
7. Verify circuit breaker CB1 (Figure 2-9) is stamped 8A.

2.5.3 System Interconnection

This paragraph details the procedure to connect the drive power cord, I/O control PCBA cables, and terminators in the daisy-chain and radial configurations. (See Figure 2-8). Verify that the site has been prepared in accordance with the site preparation information provided earlier in this section. Connect a ground strap from each control unit to system ground.

NOTE

1. *Before performing either of the following interconnection procedures, connect the ac power cord at the rear of the power control panel to the site ac power source.*
2. *Use the following cables and terminator in the interconnection procedures.*
 - Control cable, P/N 3308179-XX, maximum cumulative length - 100 feet.*
 - Read/Write cable, P/N 3308186-XX, maximum length - 50 feet.*
 - Terminator, P/N 3309833-01.*

2.5.3.1 Daisy-Chain Configuration

1. Connect control cable to control unit A and to drive connector A1J1. Connect another control cable to control unit B and to drive connector A5J1.
2. Connect read/write cable to control unit A and to drive connector A1J3. Connect another read/write cable to control unit B and to drive connector A5J3.
3. Connect control cable to drive connector A1J2 and to drive connector A1J1 of next drive in chain. Connect another control cable to drive connector A5J2 and to connector A5J1 of next drive in chain.
4. Connect terminator to drive connector A1J2 and another terminator to drive connector A5J2 of last drive in chain.

2.5.3.2 Radial Configuration

Perform the following steps for each drive in the radial configuration.

1. Connect control cable to control unit A and to drive connector A1J1. Connect another cable to control unit B and to drive connector A5J1.
2. Connect read/write cable to control unit A and to drive connector A1J3. Connect another read/write cable to control unit B and to drive connector A5J3.
3. Connect terminator to drive connector A1J2 and another terminator to drive connector A5J2.

2.6 ILLEGAL ADDRESS MAP

An illegal address map supplied with each drive informs the user of areas of media defects. A media defect is a physical characteristic of the media which results in a repetitive read error when a properly adjusted unit is operated within specific operating conditions. Valid data must not be written over known media defects; therefore, sector/track deallocation or other techniques must be utilized to avoid these areas. Table 1-1 lists the defect characteristics for the drive. The illegal address map lists head, cylinder, location (bytes from index), and length. A defective track is defined as a track containing any of the following items.

1. Two or more defects
2. False address marks

3. A defect in the format area to the extent defined by the formatting rules
4. Any single defect which causes read errors in more than one sector

Media defect-free areas are defined as follows: cylinder 0, heads 0 and 1 or any error in the logging area to the extent defined by the formatting rules.

The drive is formatted at the factory with a standard format (Figure 2-12) which is divided into two parts. The first part is a sectioned format that is normally included in the first 56 bytes following Index. The second part is an address mark format that is normally included in the next 49 bytes following Index. Format rules are as follows:

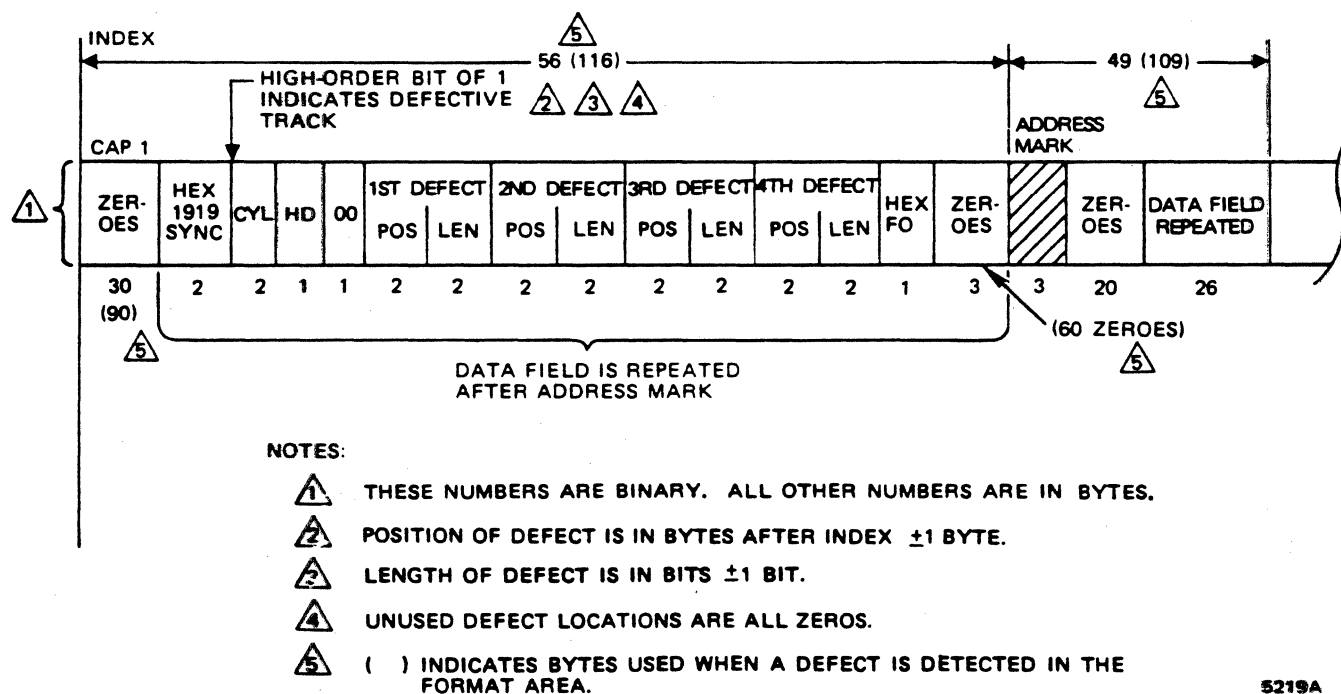
Rule 1 More than one defect on a track causes the track to be flagged as defective (refer to Rule 4). The first four media flaws are logged.

Rule 2 If the beginning of a defect is located between 15 and 56 bytes after Index, 60 bytes of zeros are added to gap 1 (90 bytes total). In this case, if any part of a defect is between bytes 70 and 165, the track is flagged as defective.

Rule 3 If the beginning of a defect is between 56 and 106 bytes after Index, 60 bytes of zeros are added immediately before the address mark. In this case, if any part of a defect is between bytes 116 and 155, the track is flagged defective.

Rule 4 If a defective track is established according to Rules 1, 2, or 3, the high-order bit of the first cylinder bytes is set to 1. Remaining information may or may not be valid.

Rule 5 The media flaws for each track are encoded in a home address format.



5219A

Figure 2-12. Capricorn Standard Defect Format

SECTION III

OPERATION

3.1 GENERAL DESCRIPTION

This section contains operating instructions for the Capricorn disk drive. Operating instructions consist of control and indicator functions, power-on procedure, operating modes, and power-off procedure.

3.2 CONTROLS AND INDICATORS

Controls and indicators for the drive are located on the operation and diagnostic control panel, on the microprocessor PCBA, and on the dual-port PCBA. The functions of these

controls and indicators are explained in the following paragraphs.

3.2.1 Operation and Diagnostic Control Panel

The operation and diagnostic control panel consists of controls and indicators that are externally visible and accessible to the operator, and of controls and indicators that are visible and accessible only after the front panel has been opened for diagnostic purposes (see Figure 3-1). Operator control and indicator functions are listed in Table 3-1. Diagnostic control and indicator functions are listed in Table 3-2.

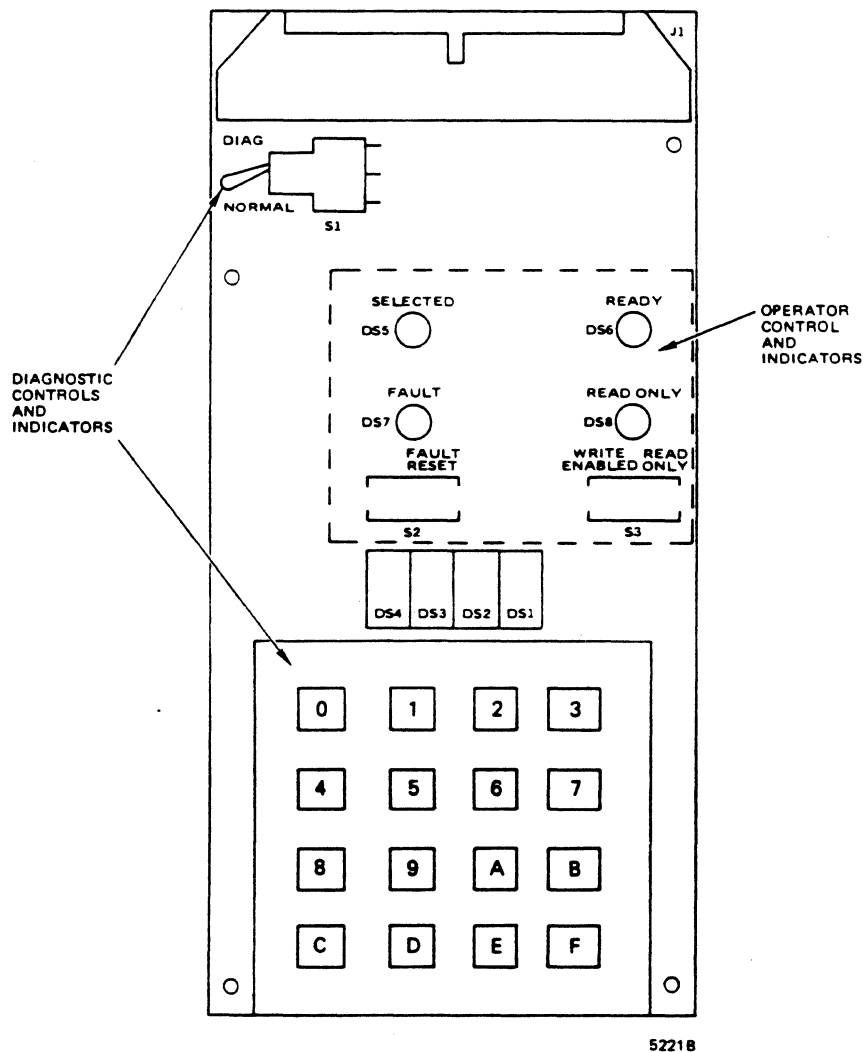


Figure 3-1. Operation and Maintenance Control Panel

Table 3-1. Operator Controls and Indicators

Control or Indicator	Desig.	Type	Function
FAULT RESET switch	A4S2	Momentary pushbutton	Resets fault latch and extinguishes Unsafe LED indicator if unsafe condition no longer exists.
READ ONLY switch	A4S3	Toggle	Disables drive from performing a write operation. NOTE: Read operations are not affected by the position of A4S3.
READ ONLY indicator	A4DS8	Yellow LED	Indicates position of READ ONLY switch.
READ indicator	A4DS6	Green LED	Indicates drive is on-line, spindle is operating at full rotational speed, and heads are positioned over data area.
SELECTED indicator	A4DS5	Green LED	Indicates drive is currently selected by control unit.
FAULT indicator	A4DS7	Red LED	Indicates unsafe condition within drive. NOTE: The error code display indicators display the error code which caused the unsafe condition.

Table 3-2. Diagnostic Controls and Indicators

Control or Indicator	Desig.	Type	Function
DIAG/NORMAL switch	A4S1	Toggle	Sets drive off-line and into diagnostic mode.
Diagnostic Key Pad		Keys 0--F (hexadecimal)	Key configuration selects diagnostic test to be executed.
Error Code Display indicators	A4DS1 to A4DS4		Display error conditions caused by drive malfunctions. NOTE: When not in Diagnostic Mode, depressing any key on the key pad resets the error display indicators.

3.2.2 Microprocessor Control Switches

Microprocessor control switches (Figure 1-1), located on the microprocessor control PCBA (A1), consist of Sectors-Per-Track, Drive Select, and Remote/Local switches. Switches A1S1 through A1S5 on the microprocessor control PCBA, shown in Figure 3-2, are accessible to the operator only after the cover of the drive has been removed.

3.2.2.1 Sectors-Per-Track Switches

The Sectors-Per-Track Switches consist of three dual-inline-pack (DIP) switches (A1S1, A1S2, and A1S3) as shown in Figure 3-2. These switches allow the operator to select from 4 to 128 sectors per track (160 to 5,040 bytes/sector). The number of sectors into which each track is divided is determined by DIP switches installed on the microprocessor control PCBA. Table 3-3 lists the sector selections available

and the applicable Sectors-Per-Track switch settings along with the respective nominal number of bytes per sector. Standard drives are set for 32 sectors by the factory.

3.2.2.2 Drive Select Switches

The Drive Select switches consist of one DIP switch (A1S4) as shown in Figure 3-2. Switch A1S4 switch positions permit the operator to assign a unique address to the disk drive. Up to sixteen combinations may be selected to allow for the individual selection of sixteen drives.

3.2.2.3 Remote/Local Switch

The REMOTE/LOCAL switch (A1S5) is a toggle switch as shown in Figure 3-2. This switch permits the drive to be powered up in sequence with other drives in a string (REMOTE position), or to be powered up independently (LOCAL position).

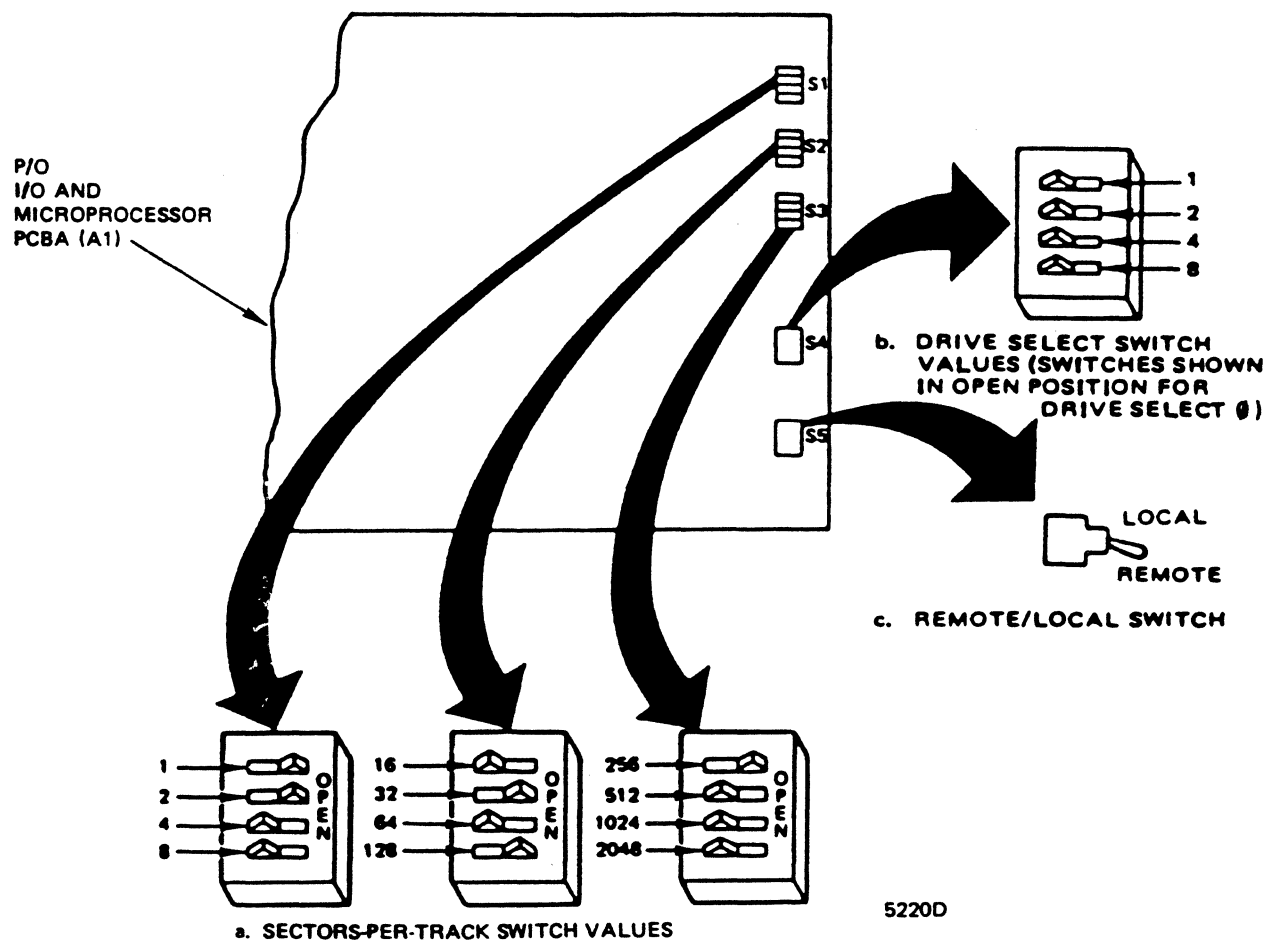


Figure 3-2. Microprocessor Control PCBA Switches

Table 3-3. Sector Selection

Sectors Per Track	Bytes Per Sector	Sectors-Per-Track Switch Hexadecimal Setting		
		A1S3	A1S2	A1S1
4	5,040	D	1	F
5	4,032	A	7	F
6	3,360	8	B	0
7	2,880	7	7	F
8	2,520	6	8	F
9	2,239	5	D	4
10	2,016	5	3	F
11	1,831	4	C	4
12	1,680	4	5	F
13	1,549	4	0	8
14	1,440	3	B	F
15	1,344	3	7	F
16	1,260	3	4	7
17	1,185	3	1	5
18	1,119	2	E	9
19	1,060	2	C	2
20	1,008	2	9	F
21	960	2	7	F
22	915	2	6	1
23	876	2	4	7
24	840	2	2	F
25	805	2	1	8
26	774	2	0	3
27	745	1	F	0
28	720	1	D	F
29	694	1	C	E
30	672	1	B	F
31	649	1	B	0
32	630	1	A	3
33	610	1	9	6
34	592	1	8	A
35	576	1	7	F
36	559	1	7	4
37	544	1	6	A
38	529	1	6	0
39	516	1	5	7
40	504	1	4	F
41	490	1	4	6
42	480	1	3	F
43	468	1	3	7
44	457	1	3	0
45	447	1	2	9
46	438	1	2	3
47	427	1	1	C
48	420	1	1	7
49	411	1	1	1
50	402	1	0	B
51	394	1	0	6
52	387	1	0	1

Table 3-3. Sector Selection (Cont.)

Sectors Per Track	Bytes Per Sector	Sectors-Per-Track Switch Hexadecimal Setting		
		A1S3	A1S2	A1S1
53	379	0	F	C
54	372	0	F	7
55	366	0	F	3
56	360	0	E	F
57	352	0	E	A
58	346	0	E	6
59	340	0	E	2
60	336	0	D	F
61	330	0	D	B
62	324	0	D	7
63	319	0	D	4
64	315	0	D	1
65	309	0	C	D
66	304	0	C	A
67	300	0	C	7
68	295	0	C	4
69	291	0	C	1
70	288	0	B	F
71	283	0	B	C
72	279	0	B	9
73	276	0	B	7
74	271	0	B	4
75	268	0	B	2
76	264	0	A	F
77	261	0	A	D
78	258	0	A	B
79	255	0	A	9
80	252	0	A	7
81	247	0	A	4
82	244	0	A	2
83	241	0	A	0
84	240	0	9	F
85	237	0	9	D
86	234	0	9	B
87	231	0	9	9
88	228	0	9	7
89	226	0	9	6
90	223	0	9	4
91	220	0	9	2
92	219	0	9	1
93	216	0	8	F
94	213	0	8	D
95	211	0	8	C
96	210	0	8	B
97	207	0	8	9
98	205	0	8	8
99	202	0	8	6

Table 3-3. Sector Selection (Cont.)

Sectors Per Track	Bytes Per Sector	Sectors-Per-Track Switch Hexadecimal Setting		
		A1S3	A1S2	A1S1
100	201	0	8	5
101	199	0	8	4
102	196	0	8	2
103	195	0	8	1
104	193	0	8	0
105	192	0	7	F
106	189	0	7	D
107	187	0	7	C
108	186	0	7	B
109	184	0	7	A
110	183	0	7	9
111	181	0	7	8
112	180	0	7	7
113	178	0	7	5
114	175	0	7	4
115	174	0	7	3
116	172	0	7	2
117	171	0	7	1
118	NOT USED	0	7	0
119	169	0	6	F
120	168	0	6	F
121	166	0	6	E
122	165	0	6	D
123	163	0	6	C
124	162	0	6	B
125	160	0	6	A
126	159	0	6	9
127	NOT USED	0	6	8
128	157	0	6	8

3.2.3 Dual-Port Controls and Indicators

The dual-port controls and indicators, shown in Figure 3-3, are located on the dual-port control PCBA (A5). Control and indicator designations and functions are listed in Table 3-4.

3.3 OPERATING INSTRUCTIONS

During the initial power-up sequence, the type of drive (Table 3-5) is displayed for a few seconds in the Error Code Display indicators A4DS1 through A4DS4 (Figure 3-1). During the power-up sequence, a number of automatic diagnostic routine sequences are performed before the drive becomes ready for system usage. A number of built-in self-tests are also performed during normal system use. When a fault is detected by these self-tests, an appropriate error code is displayed in the Error Code Display. Error codes are listed in Table 3-6.

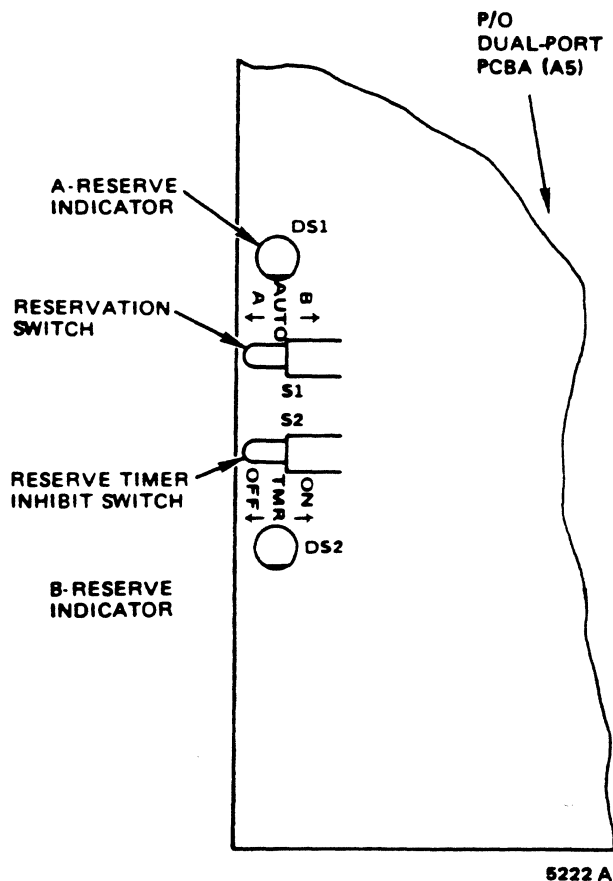


Figure 3-3. Dual-Port Option Control Switches and Indicators

Table 3-4. Dual-Port Option Controls and Indicators

Control or Indicator	Desig.	Switch Position	Function
Reservation Switch*	A5S1	A	Disables Port B; reserves drive to Port A control unit.
		B	Disables Port A; reserves drive to Port B control unit.
		AUTO	Enables device reservation logic allowing drive to be automatically reserved by control unit attempting selection.
Reserve Timer Inhibit Switch	A5S2	OFF	Inhibits reserve timer, causing drive to stay selected until specifically released by operating control unit.
		ON	Enables reserve timer to clear reserve status 500 milliseconds (nominal) following last selection. This allows alternate control unit access independent of release command. The reserve timer will not clear a priority select.
A-Reserve indicator	A5DS1		Indicates drive is reserved to Port A.
B-Reserve indicator	A5DS2		Indicates drive is reserved to Port B.

* If the drive has been automatically selected by the Port A control unit and then the Reservation switches are manually set to Disable A, the Port A reservation and selection will be immediately dropped, even if drive operations are being performed.

3.3.1 Power-Up Procedure

In the Remote mode of operation, power-up sequencing (see Figure 3-4) requires ac power on, and the LOCAL/REMOTE switch (Figure 3-2) in the REMOTE position. Applying ground to the Pick and Hold lines will cause the first drive in the sequence to power up. Once this drive is up to speed, the Pick signal is transferred to the next active drive and repeated until all active drives are powered up. Individual drives may be started and stopped once power sequencing is completed.

Table 3-5. Display of Drive Type

Display Data				Model Type	Capacity (Mbytes)	Applicable Model Specifications		Notes
A4-DS1	A4-DS2	A4-DS3	A4-DS4			Cylinder Quantity	Head Quantity	
C	3	3	0	Capricorn 330	330	1024	16	
C	1	6	5	Capricorn 165	165	823	10	Emulates CDC9730-160
1	6	5	E	Capricorn 165E	165	1645	5 Logical	Emulates Ampex DM9160

Table 3-6. Error Codes

F18 DISPLAYS ERROR LOG.

Error Code	Defect	Error Code	Defect
EC 11	ROM Failure	EC 34	Maximum Cylinder Address Exceeded
EC 12	RAM Failure	EC 42	Read Error
EC 13	Nonexisting Module	EC 43	Address Mark Read Error
EC 14	Difference Counter Fail	EC 45	Sync Error
EC 15	Seek-In Failure	EC 46	Index Error
EC 16	Seek-Out Failure	EC 52	PLO Error
EC 17	Offset-In Failure	EC 53	Write with Write-Protect Active
EC 18	Offset-Out Failure	EC 54	Write with Read Gate Active
EC 19	Servo Disable Failure	EC 55	Write with Offset Active
EC 21	Upspeed Failure	EC 56	Write without Fine Track
EC 22	Power Failure	EC 58	Multiple Head Selected
EC 31	Drifted Into Guardband	EC 59	Read/Write Unsafe
EC 32	Rezero Timeout	EC 61	Bad Entry
EC 33	Seek Incomplete		

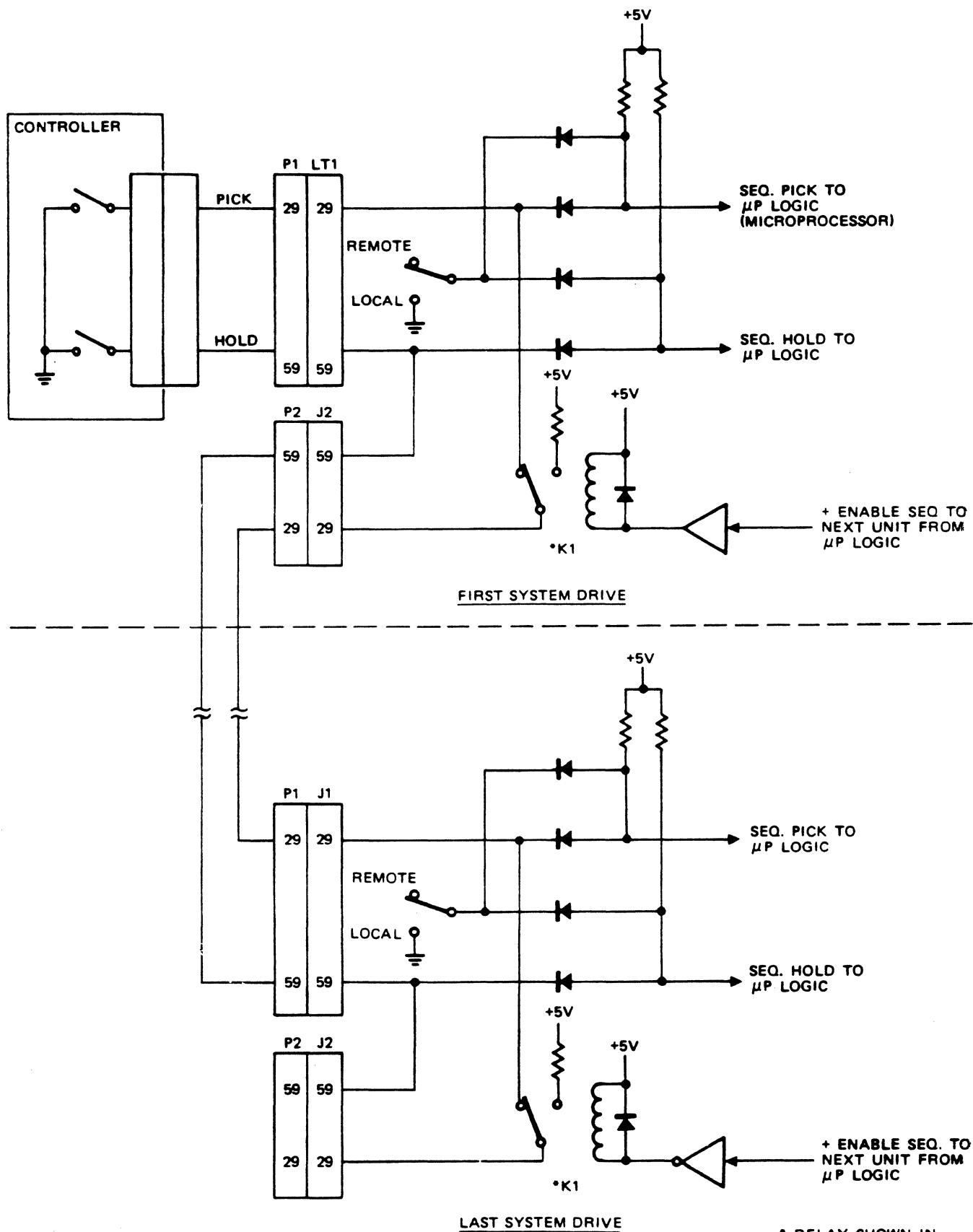
A power failure necessitates a new power-up sequence. When in Local Start mode, each drive is independently operated by its respective ac power-on switch. In the Remote mode, a Pick or Hold is considered to be present from the controller when a ground is present on "A" cable Pin 29 for Pick and Pin 59 for Hold. To initially power-up the drive in the local mode use the following procedure.

1. Place LOCAL/REMOTE switch to LOCAL position.
2. Place circuit breaker CB1 (Figure 2-9) to ON position.
3. Place DIAG/NORMAL switch (Figure 3-1) to NORMAL position.

4. Check FAULT indicator (Figure 3-1) after allowing drive to reach operating speed.
5. Check to see if READY indicator (Figure 3-1) is lit.

3.3.2 Power-Down Procedure

In the Remote mode of operation (i.e., LOCAL/REMOTE switch in REMOTE position), the power-down sequence starts either when circuit breaker CB1 is set to OFF or when the sequence power ground signal (Hold) is disabled at the controller. In the Local mode of operation (i.e., LOCAL/REMOTE switch in LOCAL position), the power-down sequence starts when circuit breaker CB1 is set to OFF. In either mode of operation, the power-off sequence retracts the heads, stops the drive motor, and extinguishes the READY indicator.



* RELAY SHOWN IN
DEENERGIZED STATE 5228B

Figure 3-4. Sequencer Power Lines

SECTION IV

THEORY OF OPERATION

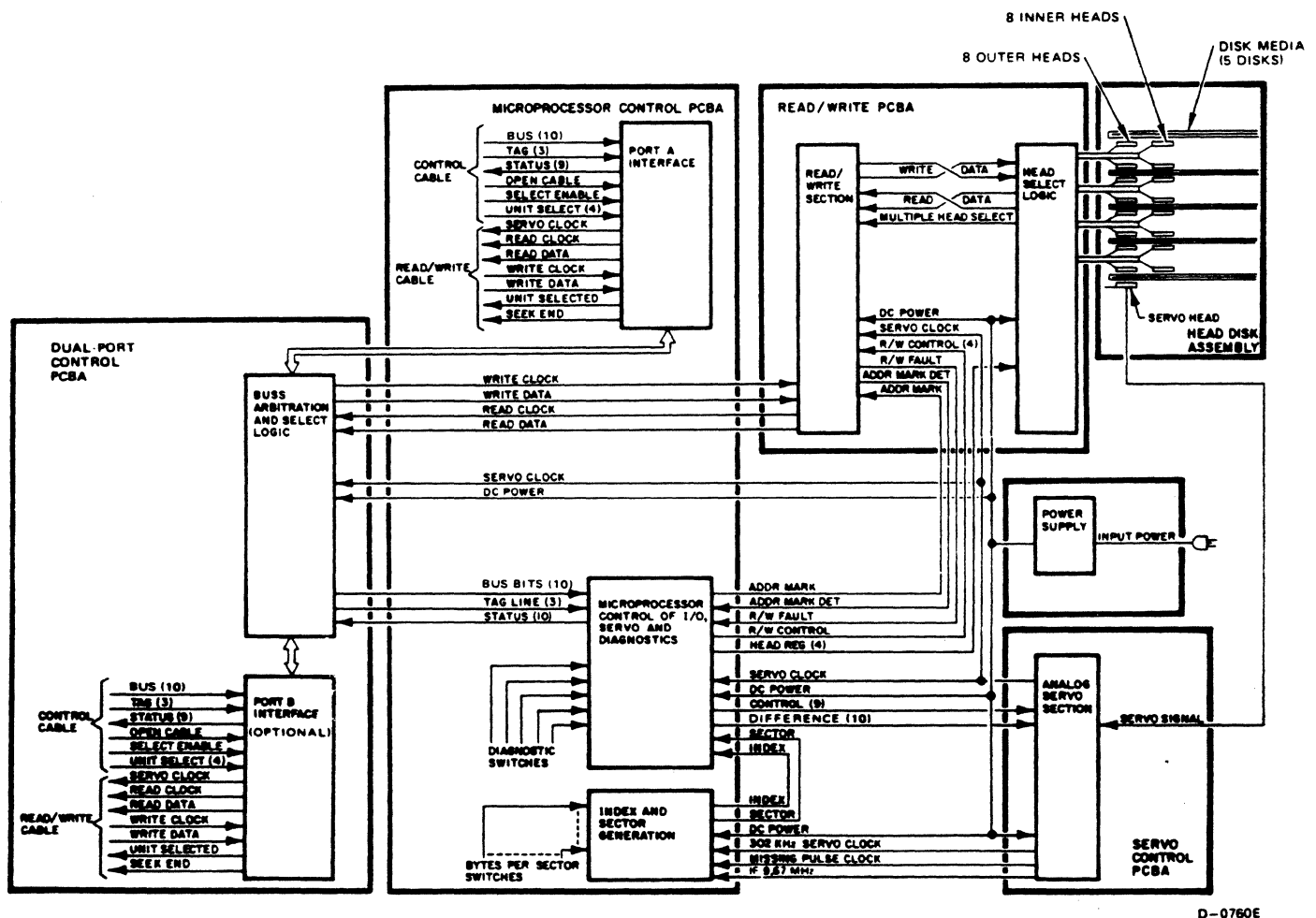
4.1 GENERAL

This section describes the theory of operation for the Capricorn 165/330 disk drive. This information provides maintenance personnel with a comprehensive understanding of the functions and operations of the drive. A brief discussion of disk recording principles is followed by a functional description of the disk drive unit that explains how the drive interfaces with the controller and describes interface signals.

The physical locations of the logics and their interconnections are shown in the detailed block diagram of Figure 4-1.

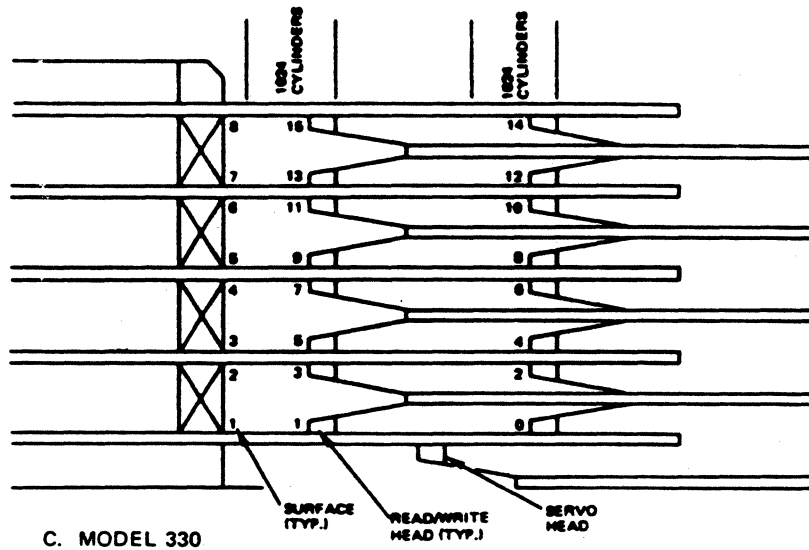
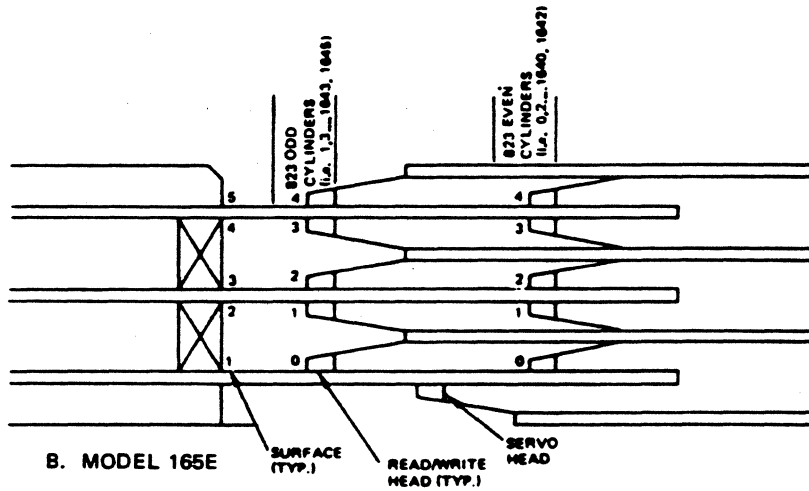
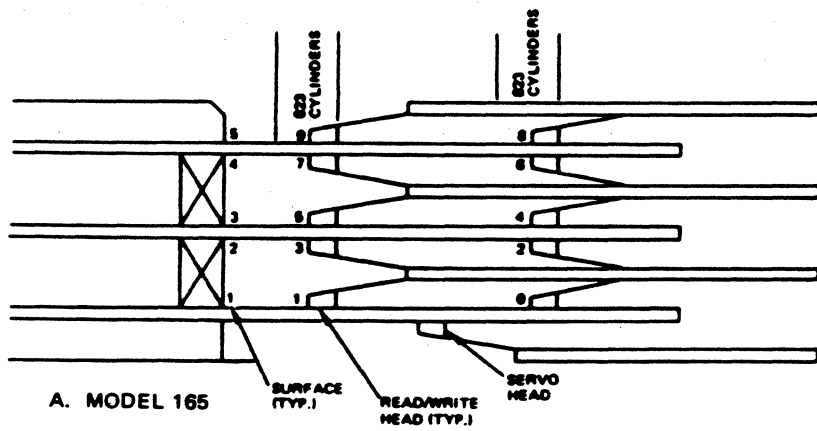
4.2 BASIC DISK PRINCIPLES

The recording medium for the drive is a stack of three 14-inch disks with five recording surfaces (Models 165 and 165E) or of five 14-inch disks with eight recording surfaces (Model 330). See Figure 4-2.



D-0760E

Figure 4-1. Capricorn Model 330 Block Diagram



52188

Figure 4-2. Surface and Head Geometry

Each disk is coated with a layer of magnetic oxide. The coating is burnished to a flatness that allows the read/write heads to fly in proximity to the surface without actual physical contact.

Data is recorded in serial fashion on concentric rings on each disk surface by holding the head in a fixed position over the rotating disk. These rings are referred to as tracks. The disk drive unit positions the heads precisely over the tracks. Corresponding track positions, both upper and lower on each disk, are referred to as one cylinder of data.

A center-tapped coil is mounted on the core of the read/write head (Figure 4-3) to perform the read/write function. The recording flux direction is controlled by energizing the center-tap connection, causing current to flow through the bifilar winding from the center tap to either one end of the coil or the other. When reading, the ends of the coil are switched to the input of the read amplifier. Data is erased by writing new data on the track. The read/write coil is mounted onto the core of the ferrite slider. As the disk rotates, it pulls a film of air around its surface. This moving air moves under the slider and exerts an upward force on the slider. A downward pressure is placed on the slider by the spring flexure of the head. The slider then flies at a point where the downward force of the load spring is equal in force to the air pressure under the head.

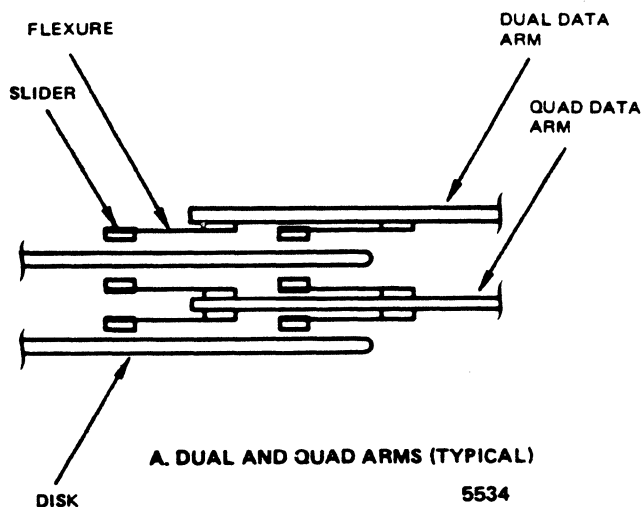


Figure 4-3. Read/Write Assembly

The nominal flying height of the head is 19 microinches at 3600 rpm. The head is closer on an inner track because the inner track portion of the disk is moving at a slower speed than the outer track portion of the disk, resulting in less air pressure on the inner track than on the outer track.

The slider is mounted to the head arm assembly via a spring gimbal-mount (Figure 4-4). This allows the flying attitude of the slider to vary slightly so that it can follow minor surface variations without contacting the disk surface.

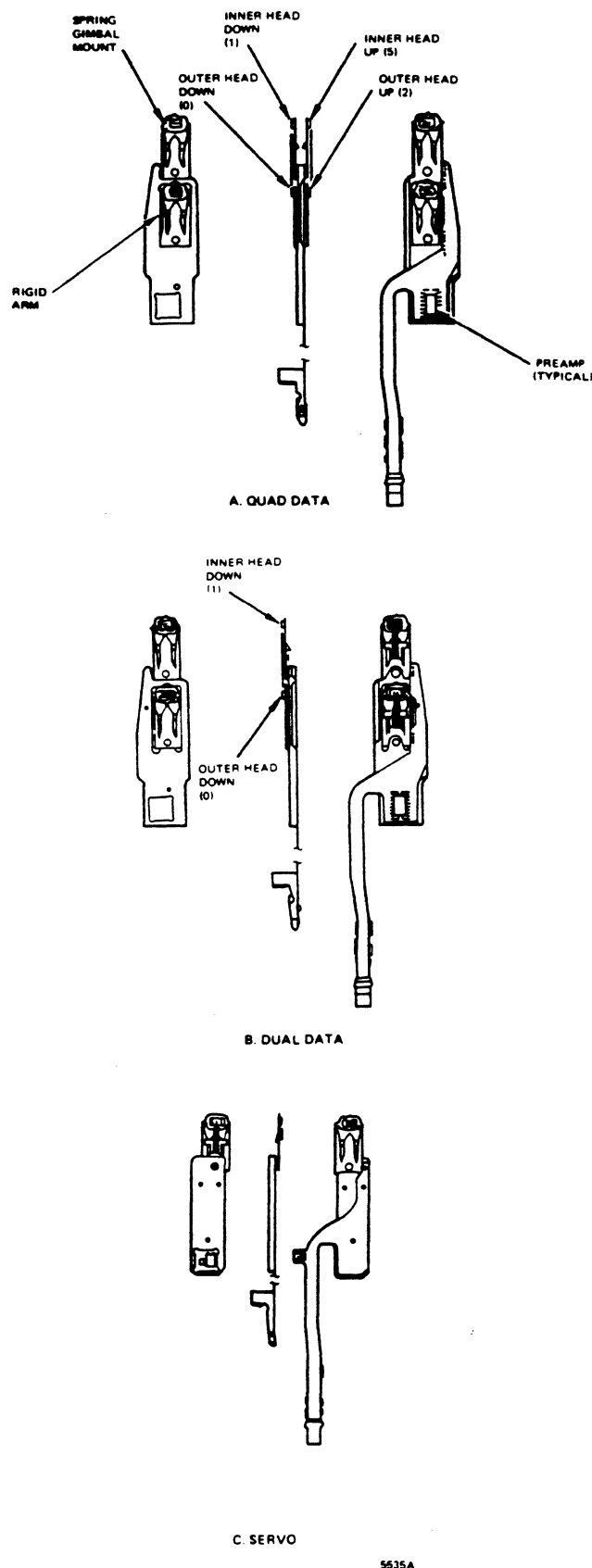


Figure 4-4. Head Arm Assemblies

All heads are mounted on a carriage so that the heads and carriage move as one unit. The carriage moves the heads radially over the disk's surfaces. All the heads are positioned to the same cylinder at any given time. The servo disk provides the servo system with the exact track information so that the head gaps may be positioned precisely over any of the tracks on a disk surface.

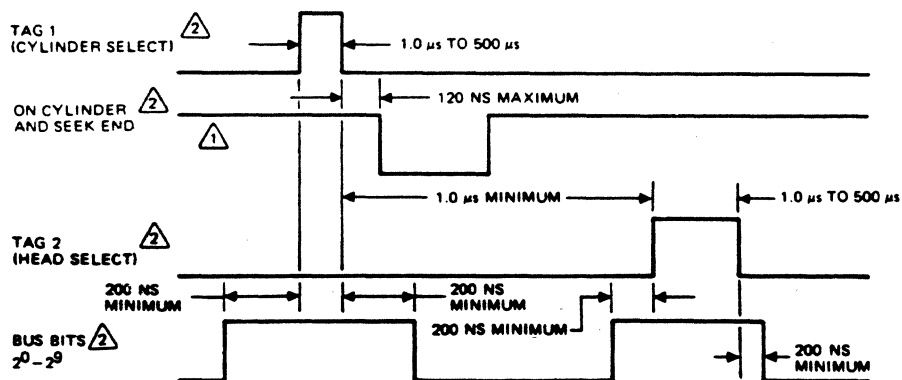
selection lines are used to provide the logical connection of a disk drive to the control unit. Three function tags are used to perform cylinder select, head select and control select functions as listed in Table 4-1. Minimum tag/bus timing is shown in Figure 4-5 and movable head tag/bus timing is shown in Figure 4-6. The following paragraphs define control interface signals.

4.3 CONTROL AND STATUS LINES

Most control and status data is exchanged between drive and control unit via the control cable (paragraph 2.5.1.1). Six

Table 4-1. Function Tag/Bus-Out Definitions

Bus-Out Bits	Function Decode			
	Cylinder Select Tag	Head Select Tag	Control Select Tag	Unit Select
0	CAR 2 ⁰	HAR 2 ⁰	Write Gate	Priority Select
1	CAR 2 ¹	HAR 2 ¹	Read Gate	
2	CAR 2 ²	HAR 2 ²	Offset Forward (+)	
3	CAR 2 ³	HAR 2 ²	Offset Reverse (-)	
4	CAR 2 ⁴	HAR 2 ³	Fault Clear	
5	CAR 2 ⁵		Address Mark Enable	
6	CAR 2 ⁶		Rezero	
7	CAR 2 ⁷		Data Strobe Early	
8	CAR 2 ⁸		Data Strobe Late	
9	CAR 2 ⁹		Release	
10	CAR 2 ¹⁰			

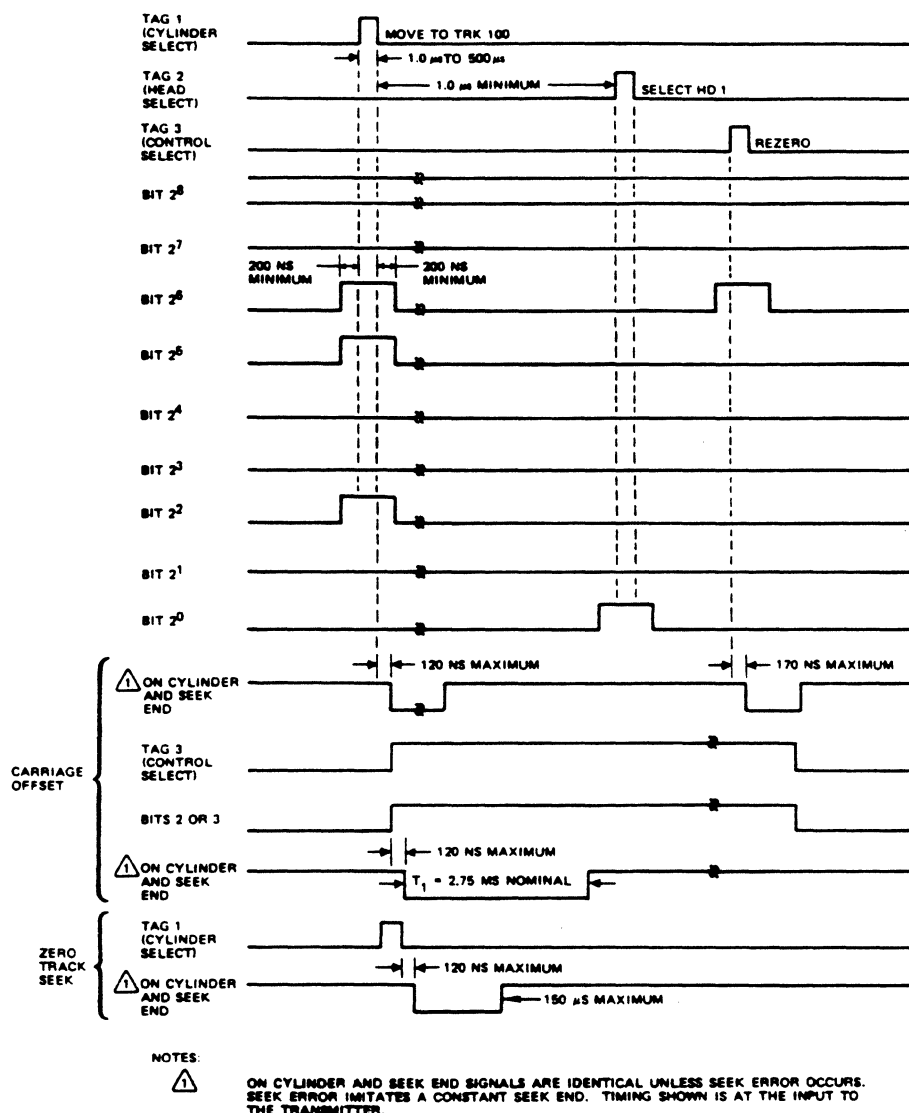


NOTES:

- ① TIMING SHOWN IS AT THE INPUT TO THE TRANSMITTER.
- ② TAG 1 AND TAG 2 MAY BE ISSUED IN EITHER ORDER PROVIDING 1.0 μs MINIMUM TIMING IS ALLOWED BETWEEN COMMANDS.

5224A

Figure 4-5. Minimum Tag/Bus Timing



5226A

Figure 4-6. Movable Head Tag/Bus Timing

4.3.1 Device Enable (Open Cable Detector)

When active, Device Enable (Open Cable Detector) signal enables the receivers and drivers, and allows drive selection and operation from the control unit. The absence of this signal disables the receivers and drivers, and all control-unit-generated control functions, including write.

4.3.2 Select Enable (Unit Select Tag)

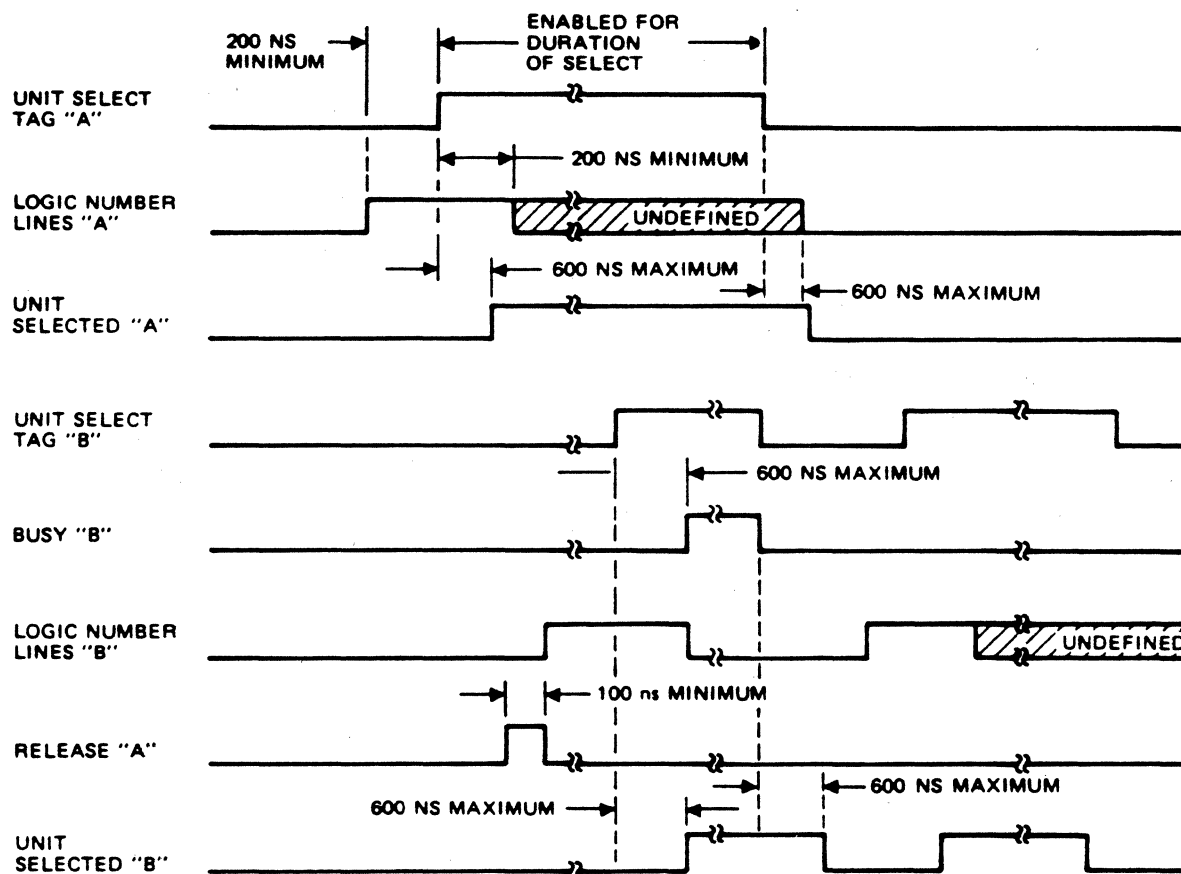
The leading edge of Select Enable causes the drive to become selected if the select number on the Device Select lines compares with the address set in the drive. Only the drive with the same number as that being sent by the control unit on the Device Select lines is selected. Selection of the drive occurs within 600 nanoseconds maximum after the leading edge of the Select Enable signal. The Select Enable signal (as well as the Device Select lines) must be held active during the entire period of selection.

4.3.3 Unit Select Lines (2⁰, 2¹, 2², 2³)

Four Unit Select lines are binary decoded to select one of sixteen disk drives on the control cable. The unit select address is determined by a four-switch DIP pack. The Device Select lines should be stable 200 nanoseconds before the leading edge of the Select Enable signal (Figure 4-7).

4.3.4 Tag 1 (Cylinder Select)

Tag 1 (the Cylinder Select tag line) transfers the cylinder address on the control bus line (bits 0 through 9) to the control logic. The control logic computes the direction and difference to the target cylinder, initiates the seek if difference > 0, and loads the CAR with the new address.



5223A

Figure 4-7. Logic Number Select and Timing Diagram

4.3.5 Tag 2 (Head Select)

Tag 2 (the Head Select signal) when active, gates the four low-order bits of the bus-out lines to the Head Address Register (HAR).

4.3.6 Tag 3 (Control Select)

Tag 3 (the Control Select signal), when active, allows ten bus-out bits to be used as control operations in a selected disk drive. The significance of the bus-out bits with the control select active is as follows.

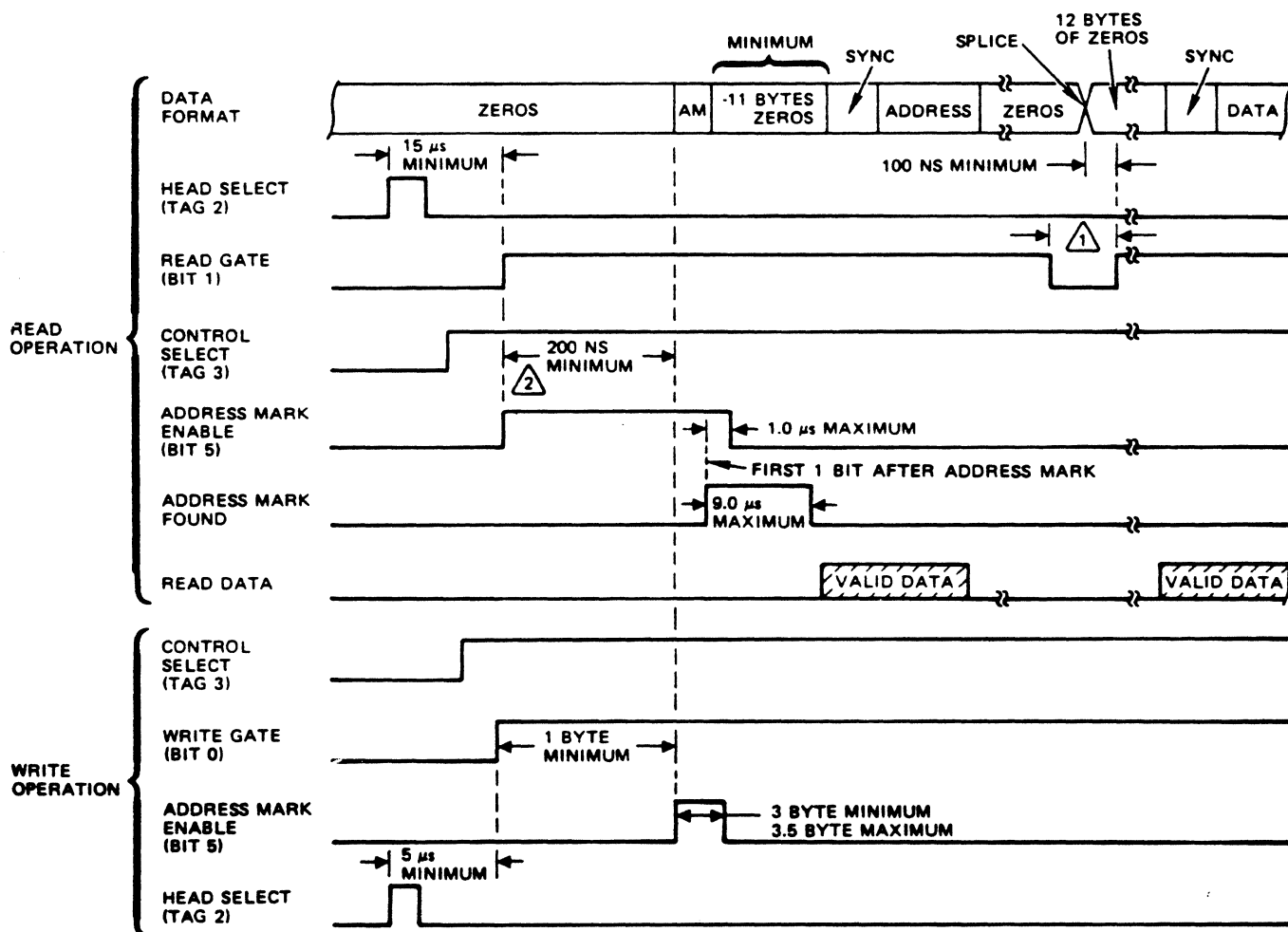
1. BUS-OUT 0 -- WRITE GATE

The Write Gate signal (Figures 4-8 and 4-9) enables the write circuitry to convert the digitized information on the write data line to current reversals in the

read/write head, thereby recording information on a selected track on the disk stack. The Write Gate signal causes an unsafe condition to exist if Write Transitions, Write Current, Write Oscillator, Write Protect, Offset, PLO, and Fine Track Signals are not correct or do not occur at the correct time.

2. BUS-OUT 1 -- READ GATE

The Read Gate signal (Figures 4-8 and 4-9) enables the read circuitry to convert the MFM information recorded on a given track to NRZ data which is gated through the read data line back to the control unit.

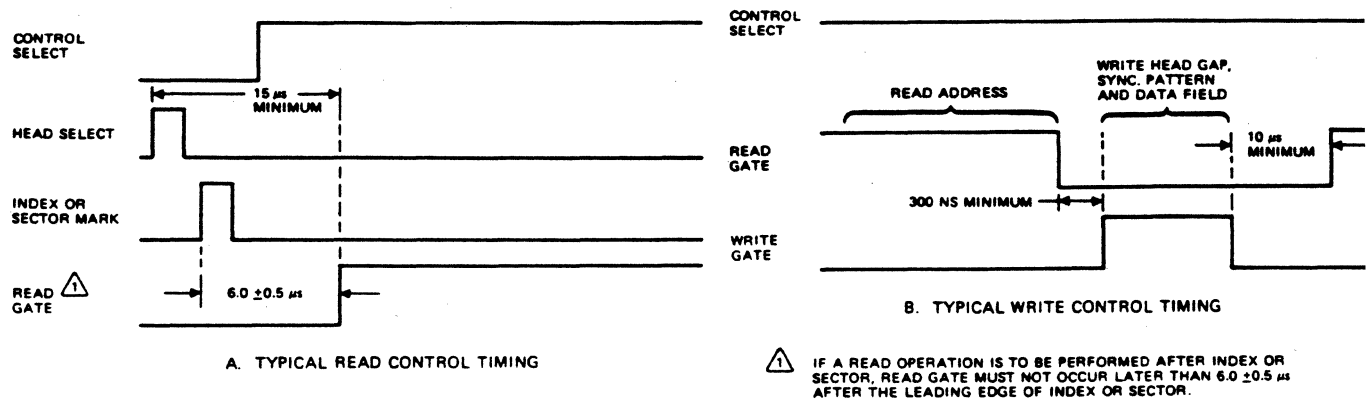


NOTES:

① READ GATE MUST BE DROPPED PRIOR TO THE WRITE SPLICE. IT MUST BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 10 BYTES OF ZERO BITS REMAINING IN THE SYNC FIELD. 12 BYTE EXAMPLE CONSISTS OF ONE BYTE FOR WRITE SPLICE AND 11 BYTES FOR PLO SYNC.

② ADDRESS MARK ENABLE SHOULD OCCUR SIMULTANEOUSLY WITH READ GATE.

Figure 4-8. Typical Read/Write Timing with Address Mark



5227

Figure 4-9. Control Timing

3. BUS-OUT 2 -- OFFSET FORWARD (IN)

The Offset Forward signal moves the head positioner 60 microinches toward the spindle from the on-track position. This command causes the loss of On Cylinder status for 2.75 milliseconds. This command, if active with Write Gate, causes a fault condition which disables the read/write circuitry.

4. BUS-OUT 3 -- OFFSET REVERSE (OUT)

The Offset Reverse signal moves the head positioner 60 microinches away from the spindle from the on-track position. This command causes the loss of On Cylinder status for 2.75 milliseconds. This command, if active with Write Gate, causes a fault condition which disables the read/write circuitry.

5. BUS-OUT 4 -- FAULT (UNSAFE) RESET

The Fault Reset signal clears the Fault (Read/Write Unsafe) condition. This command must be active for 100 nanoseconds minimum.

6. BUS-OUT 5 -- ADDRESS MARK ENABLE

The Address Mark Enable signal (Figure 4-8), when used in conjunction with Write Gate, allows the control unit to erase portions of a given track without causing an unsafe condition due to lack of write transitions. The Address Mark Enable signal, when used in conjunction with the Read Gate, causes a biasing of the read

circuitry to allow the control unit to search for erased areas on a given track. This command allows the control unit to use a variable-length record format.

7. BUS-OUT 6 -- REZERO

The Rezero signal causes the head positioner to reposition to cylinder 0 and resets the HAR and clears the seek error conditions. The command causes loss of On Cylinder until the heads are positioned at cylinder 0. The command must be active 250 nanoseconds minimum, 1.0 millisecond maximum.

8. BUS-OUT 7 -- DATA STROBE EARLY

The Data Strobe Early signal causes the clocked data separator to strobe the read data 5 nanoseconds (nominal) earlier than normal.

9. BUS-OUT 8 -- DATA STROBE LATE

The Data Strobe Late signal causes the clocked data separator to strobe the read data 5 nanoseconds (nominal) later than normal.

10. BUS-OUT 9 RELEASE COMMAND

The Release command (applicable for the optional dual-port drive) is transmitted by the using control unit to release its reservation of the drive, making the drive immediately available to the partner control unit.

4.3.7 Index

The index line is a status indicator that, when active, indicates the reference point or index area is passing under the heads. The index point is a pulse which occurs once per revolution of

the disk stack and is nominally 2.5 ± 0.3 microseconds in duration. The device must be selected to enable this line (see Figure 4-10). Timing integrity is maintained throughout seek and rezero operations.

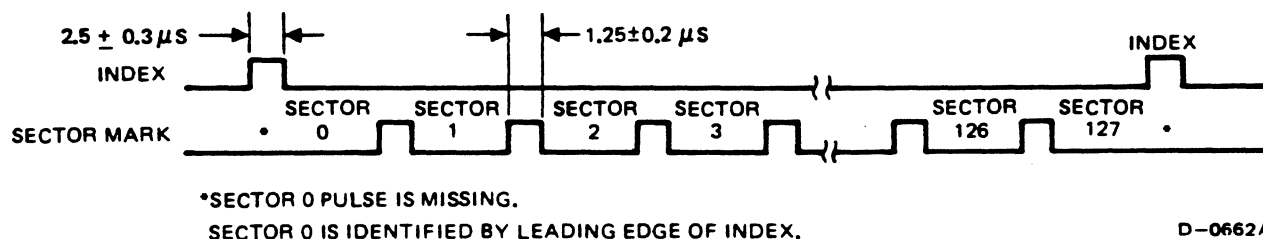


Figure 4-10. Index and Sector Timing

4.3.8 Sector Mark

The Sector Mark line establishes rotational reference points along a given track on the disk stack. Each track may be divided into sectors ranging from 4 to 128 with the initial or 0 sector starting coincident with the index point. (Note that no Sector Mark pulse is transmitted for sector 0. The index pulse may be considered the sector 0 pulse.) Sector Mark is a pulse nominally 1.25 ± 0.2 microseconds in duration. The device must be selected to enable this line (see Figure 4-10).

4.3.9 Fault (Read/Write Unsafe)

The Fault signal, when active, indicates that a Fault condition has occurred within the drive, which makes the reliability of read and write operations questionable. The Fault condition disables the read and write sections of the drive to prevent inadvertent destruction of recorded data. This condition also causes the Ready signal to deactivate and extinguish the Ready LED located on front OCP. (On Cylinder and Seek End remain unchanged.) Conditions which cause a fault are listed in Table 4-2.

Table 4-2. Fault Conditions

Set Condition	Fault Signal Set Cause
Read/Write PCBA power failure	Dc voltage fault
Head select fault	Multiple heads selected
Write control error	1. Write command and drive write protected 2. Write command and track offset 3. Write command and not find track 4. Write command and read command concurrent 5. Write command and write disable
VFO error	Write command and write clock error
Write Current	1. Write command and no write current present 2. No write command and write current present
Write Transition	Write command and not address mark and no write transitions

The Fault signal is reset by:

1. A controller-initiated reset
2. The FAULT RESET switch on the front OCP
3. The power-up reset which occurs when power is initially applied

4.3.10 Seek Error

Status signal Seek Error indicates one of the following:

1. Drive failed to complete a seek operation within 100 milliseconds.
2. Drive failed to complete a head load, rezero operation within 700 milliseconds.
3. Either outer or inner guardbands are detected while performing a seek operation.
4. Power Failure condition occurred.
5. Drive received an illegal address (>1023 for Model 330 or >822 for Model 165).

The Seek Error condition causes the servo to be disabled and forces the Seek End signal active. The Seek Error condition may be cleared by a Rezero command from the control unit, from the maintenance and control panel, or by a power-down operation. The drive must be selected to gate the Seek Error signal to the control unit.

4.3.11 On Cylinder

Status signal On Cylinder generally indicates that the head positioner is stationary, that it is positioned over a defined track, and that it is ready to perform the next operation. An exception is that On Cylinder is forced active when Seek Error is active. Any motion operation causes the loss of On Cylinder until the heads are repositioned. Such motion operations include seeks and rezero. Additionally, the On Cylinder status will be inactive whenever the heads are in a landing zone. During offset operations, the On Cylinder signal drops low for nominally 2.75 milliseconds. This line also goes low for 150 microseconds maximum on a zero track seek.

4.3.12 Unit Ready

Status signal Unit Ready indicates that:

1. Disk stack is up to speed
2. Heads are located over a data track
3. No Fault (Unsafe) condition exists within the drive

4.3.13 Write Protected

Signal Write Protected indicates the READ ONLY switch is on and the recording of information on the disk stack is inhibited. Activating Write Gate with the protect status active causes read/write unsafe and fault to be issued.

4.3.14 Address Mark Found

Signal Address Mark Found is activated by the combination of read gate, address mark enable, and the absence of data for approximately 24-bit cell times. This line is active for 9.0 microseconds.

The Address Mark Found capability is incorporated as a part of the NRZ read circuit and enhances the use of variable-length records. The drive performs the Address Mark Search and recognition function for the control unit. The control unit, by raising the Address Mark Enable signal along with Read Gate, causes the drive to search for the next dc erased area (16 bits or greater = Address Mark) on the track. During this search period, no data passes on the read data line. When the Address Mark is located, the drive raises the Address Mark found pulse. The control unit then drops the Address Mark Enable and continues to monitor the Address Mark Found line. When Address Mark Found drops to its inactive state, valid read data is available on the read data line. A minimum of 9.0 microseconds of zeros must be used after address marks to ensure proper synchronization of the data separator.

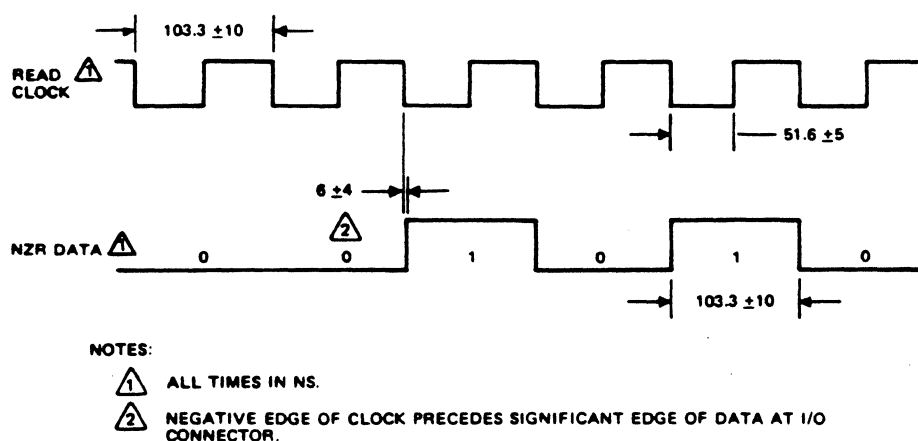
NOTE

It may be possible for the drive to issue a false Address Mark Found during an Address Mark Search due to a media defect.

4.3.15 Power Sequencing

Power sequencing (see Figure 3-4) requires ac power on, and the REMOTE START switch (switch selectable in device) in the REMOTE position. Applying ground to the Pick and Hold lines causes the first device in the sequence to power up. Once this device is up to speed, the Pick signal is transferred to the next active device and repeated until all active devices are powered up. Individual devices may be started and stopped once power sequencing is completed.

A power failure necessitates a new power-up sequence. When in Local Start mode, each device is independently operated by its respective ac power-on switch. In the Remote mode, a Pick or Hold is considered to be present from the controller when a ground is present on "A" cable Pin 29 for Pick and Pin 59 for Hold.



5229 A

Figure 4-11. Read Clock Timing

4.4 READ/WRITE LINES

The read/write cable (paragraph 2.5.1.2) transfers all NRZ data and clock signals between the control unit (CU) and the disk drive. The following paragraphs define read/write interface signals.

4.4.1 Read Clock

Signal Read Clock provides the timing to allow the sampling of the clocked read data which appears on the read data line. This signal is transmitted continuously, and is in phase sync within 9 microseconds after Read Gate.

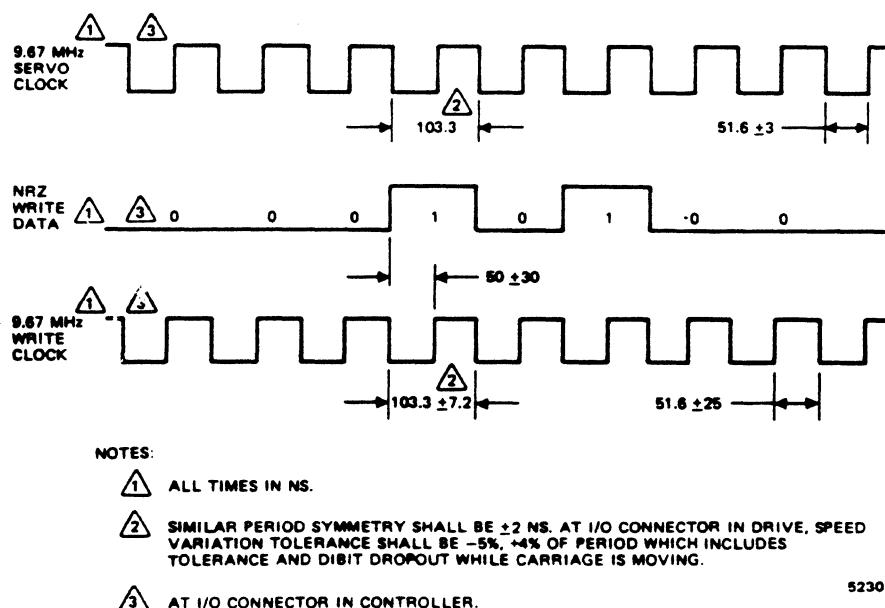
4.4.2 Read Data

The clocked Read Data signal (NRZ) is transmitted to the control unit on the Read Data line (Figure 4-11). The clocked

read data is controlled by read gate, and in order to synchronize the data separator properly, read gate must be asserted in a known field of zeros. From initiation of read gate, a minimum of 9.0 microseconds of zeros is required to permit synchronization of the data separator.

4.4.3 Write Clock

Signal Write Clock is used in the disk drive to synchronize the clocked write data from the control unit (Figure 4-12). Write Clock may be the servo signal retransmitted back to the disk drive; however, the clocked write data must be synchronized with the write oscillator in the disk drive. Write clock must be transmitted at 250 nanoseconds before the activation of Write Gate and may be transmitted continuously, following selection of the drive.



5230 A

Figure 4-12. Write Clock Timing

4.4.4 Write Data

The Clocked Write Data signal is transmitted from the control on the write data line and must be synchronized with the write clock line as shown in Figure 4-12. The write gate command controls the writing of MFM data on the disk stack. When used in conjunction with Write Gate, the address mark command inhibits the writing of bits on the disk stack (dc erases), and thereby generates an address mark for the duration of the address mark command. The address mark command leading and trailing edges must coincide with the negative edge of the Write Clock. The clocked write data must be held in the zero state for the duration of the address mark command.

4.4.5 Servo Clock

The Servo Clock signal is developed within the drive from the signal read by the servo head from the surface of the disk stack (Figure 4-12). The nominal frequency of the Servo Clock signal is 9.677 MHz when track-following. Since the Servo Clock signal is derived from the prerecorded signal on the disk stack, variations in rotational speed are reflected in frequency changes of the servo clock. The servo clock then provides to the control unit a method of synchronizing the Write Data signal with the actual speed of the disk. The servo clock is a symmetrical square wave with a nominal period of 103 nanoseconds.

The control unit examines this from each drive in the system after raising the Select Enable line to ensure that no more than one drive responded with a select. Read/write data and clocks may also be gated by this line.

4.4.6 Seek End

The Seek End signal is the same as the On Cylinder signal, with the exception that it is in the read/write cable and it is not gated by drive select. Its change from the inactive to the active state may be used by the control unit as a flag or interrupt that indicates the drive has completed an operation and requires the control unit's attention. The signal is normally in the active state. Changes from the state are as follows:

1. Seek End (and On Cylinder) drops after the initialization of a seek operation and remains low until the seek completes normally or a seek error (seek incomplete) condition occurs.
2. Seek End (and On Cylinder) drops after initialization of a rezero operation and remains low until the rezero completes normally or a seek error (seek incomplete) condition occurs.
3. During offset operations, Seek End (and On Cylinder) drops for approximately 2.75 milliseconds.

4. The Seek End (and On Cylinder) signal goes inactive and remains there when the heads go into landing zone. The signal activates again when the heads are on cylinder.
5. The Seek End signal also drops for 150 microseconds maximum on a zero track seek.

4.4.7 Index

Signal Index (paragraph 4.3.7) is available on the read/write cable to the control unit at all times, except during diagnostics. As an option, the Index signal for the read/write cable can be deleted.

4.4.8 Sector Mark

Signal Sector Mark (paragraph 4.3.8) is available on the read/write cable to the control unit at all times, except during diagnostics. As an option, the Sector Mark signal for the read/write cable can be deleted.

4.4.9 Selected

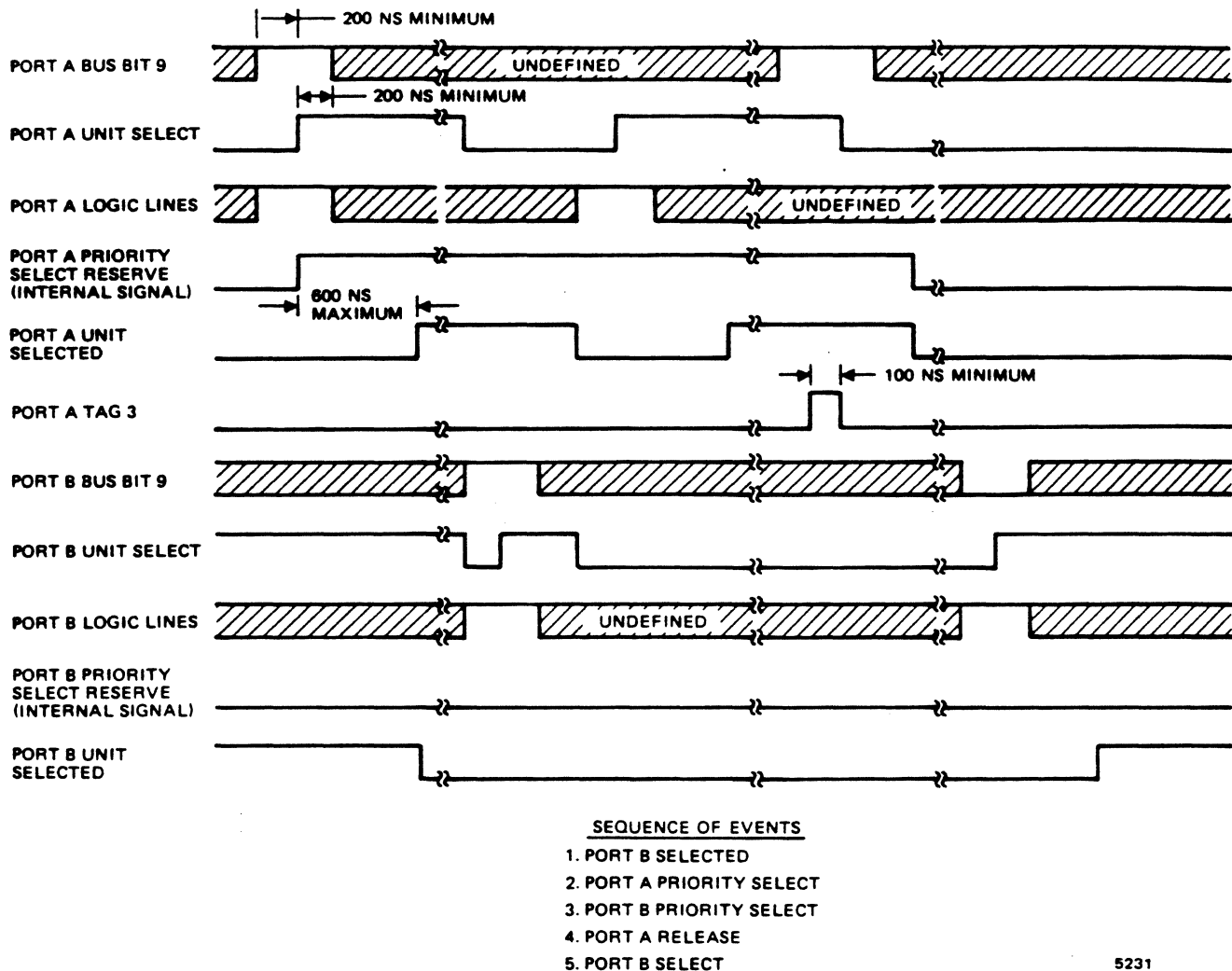
Signal Selected is transmitted from the drive to the control unit, following a successful compare of the address on the Device Select lines with the address internally set in the drive. This line activates 600 nanoseconds after the drive receives the leading edge of the Select Enable line. The control unit examines this line from each drive in the system after raising the Select Enable line to ensure that no more than one drive responded with signal Selected.

4.5 DUAL-PORT INTERFACE (OPTIONAL)

The dual-port interface permits the drive to communicate with two control units through two identical interfaces designated as Port A and Port B. The dual-port interface has two additional commands and one additional status line in the control cable. The read/write cable has the same signals as the standard cable for the drive. Pin assignments and signal polarities are the same as those listed in Table 2-4. A brief description of the dual-port interface is provided in the following paragraphs.

4.5.1 Release Command

This command (bus-out bit 9 and the control select tag), transmitted to the drive, releases controller reserve and priority select in the drive, making alternate control unit access possible (Figure 4-13).



5231

Figure 4-13. Sample Priority Select Timing

4.5.2 Priority Select Signal

This signal is active when bus-out bit 9 is active coincident with the leading edge of the Unit Select signal and the desired logic number on the unit select number lines (Figure 4-13). Setting Priority Select forces the drive to become unconditionally selected and absolutely reserved by the issuing control unit if the Reservation switch is off and the partner control unit does not have a priority select. If the opposite control unit does not have an active priority select, but does have a select active, any operation is immediately terminated and the control unit force-released. This function enables a control unit to force a partner control unit and system off the drive in cases of urgency or suspected

malfunction. Following a priority select on one channel, all interfaces are inhibited on the opposite channel including Unit Selected and Busy.

4.5.3 Busy Status Signal

If the drive is selected and/or reserved by one control unit, the Busy signal is active on the control cable and the Selected signal is active on the read/write cable to the partner control unit attempting the select. These signals are issued from the drive within 600 nanoseconds following receipt of the selection, and remain at this status until Unit Select is dropped or the drive is no longer busy.

4.6 INTERFACE DEFINITION

The drive utilizes industry-standard differential line transmitters and line receivers on all interface lines to provide a high-speed, balanced, terminated transmission network which allows the use of long lines. The transmitter inputs and the receiver outputs are DTL/TTL-compatible logic levels. The transmission network provides for ± 3 volts of common mode noise rejection while offering low propagation delays through both the transmitters and receivers. Figure 4-14 illustrates a typical control-unit-to-drive control or status transmission line. Figure 4-15 illustrates a typical data or clock transmission line.

4.6.1 Line Transmitter Characteristics

The line transmitters used for communication between a control unit and the disk drive are capable of sinking 12 ± 3 milliamperes in the ON state, and a maximum of 100 microamperes in the OFF state. Table 4-3 shows the output relationship to the various input combinations for the line transmitters.

The propagation delay through the driver does not exceed 15 nanoseconds with a 50-ohm load at 50 percent signal levels.

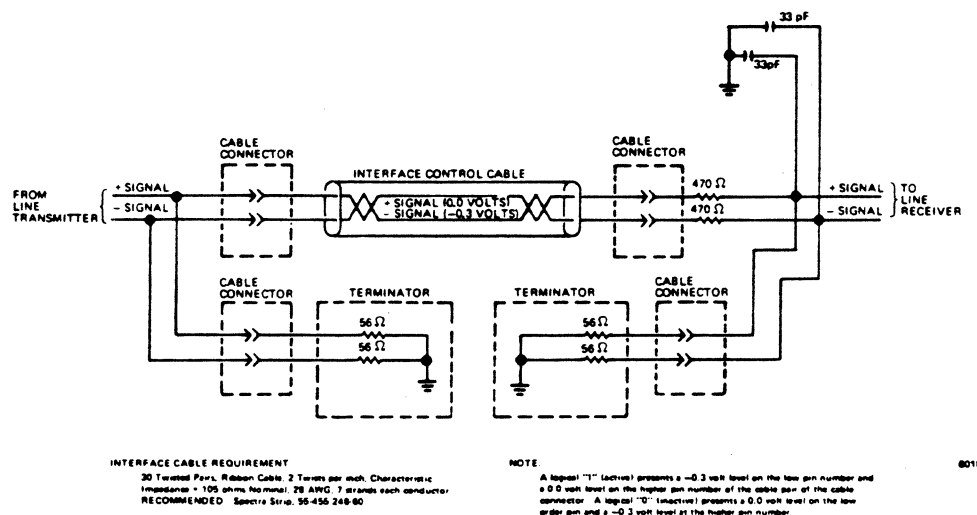


Figure 4-14. Control or Status Transmission Line

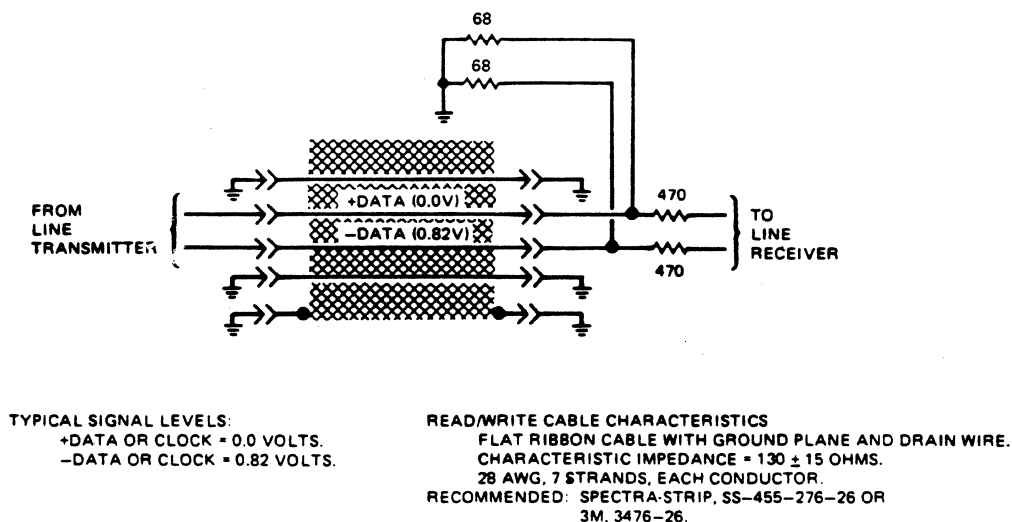


Figure 4-15. Data or Clock Transmission Line

Table 4-3. Transmitter Truth Table

Logic Inputs		Inhibit Inputs		Outputs	
Signal	Enable	Inhibit 1	Inhibit 2	Y	Z
1 or 0	1 or 0	0	1 or 0	OFF	OFF
1 or 0	1 or 0	1 or 0	0	OFF	OFF
0	1 or 0	1	1	ON	OFF
1 or 0	0	1	1	ON	OFF
1	1	1	1	OFF	ON

Inhibitor inputs should be held high on line transmitters in the control unit, since the line levels are indeterminate when inhibited and have no significance to the drive interface. Line transmitters are enabled in the disk drive only when the drive is selected.

4.6.2 Line Receiver Characteristics

The line receivers used for communication between a control unit and the disk drive are capable of detecting a differential signal of greater than ± 25 millivolts and less than ± 5 volts. The receivers are capable of detecting the polarity of the differential signal, with up to ± 3 volts of common mode voltage on the inputs. Table 4-4 shows the respective receiver outputs for the various input combinations. The propagation delay through the receiver does not exceed 25 nanoseconds when driving a 390-ohm load in parallel with 50 picofarads measured at the 50 percent signal levels with a ± 100 -millivolt input signal.

4.6.3 Line Terminator

1. All control signal lines must be terminated with 56-ohm resistors from each side of the balanced differential line to ground at both the transmitting and receiving ends. At the drive end of the cable, the terminator resistors are located in a terminator plug attached to the Control cable output connector of the last drive in the string.
2. The Read Data, Write Data, Servo Clock, and Write Clock lines are terminated with 68-ohm resistors from each side of the differential line to ground at the receiving end only. (Other control and status lines in the read/write cable must be terminated at both ends of the cable with 56-ohm resistors from each side of the differential line to ground.)

Table 4-4. Receiver Truth Table

Differential Inputs	Enables		Output
	Enable 1	Enable 2	
$V_{AB} \geq 25\text{MV}$	1 or 0	1 or 0	1
$-25\text{MV} \geq V_{AB} \geq -25\text{MV}$	1 or 0	0	1
	0	1 or 0	1
	1	1	Undefined
$V_{BA} \geq 25\text{MV}$	1 or 0	0	1
	0	1 or 0	1
	1	1	0

SECTION V

MAINTENANCE

5.1 GENERAL

This section provides information necessary for the maintenance of the Capricorn 165/330 disk drive. Included are routine adjustments and alignments, removal and replacement procedures for major subassemblies, and a description of the built-in diagnostics. No special tools or test equipment are required for the performance of routine adjustments and alignments.

5.2 DIAGNOSTICS

The Capricorn diagnostics are divided into three sections: 1) Power-Up Diagnostics, 2) Operational Error, and 3) Internal Diagnostics.

5.2.1 Power-Up Diagnostics

During the power-up sequence in the drive, a number of automatic diagnostic routine sequences are performed before the drive becomes ready for system usage. During the power-up sequence, the type of drive is displayed for a few seconds in the error code display (Table 5-1). When a fault occurs, an appropriate error code is displayed in the fault indicators. Table 5-2 lists the description of these tests and the applicable error code.

Table 5-1. Type-of-Drive Display

DISPLAY	MODEL TYPE	CAPACITY	CYLINDERS	HEADS
C330	330	330 MB	1024	16
C165	165	165 MB	823 Emulates CDC 9730-160	10
165E	165E	165 MB	1645 Emulates Ampex DM9160	5 Logical

Table 5-2. Power-Up Error Code Descriptions

ERROR CODE	DESCRIPTION
EC 11	ROM CHECK Reads each byte of data from ROM and adds this to the next byte of data until the second to last byte. The sum is then compared to the last byte of data. If the ROM is good, the sum should be equal to the last byte.
EC 12	RAM CHECK Writes a data pattern of 10101010 to RAM, performs a shift function, then reads the data pattern back. Result should be 01010101; if not, then the RAM is bad. If good, then a pattern of all zeros is written to RAM.
EC 13	IDENTIFY HDA A 4-bit binary code is read from the HDA to determine the module type.
EC 14	DIFFERENCE COUNTER CHECK A count equivalent to difference = 0 is loaded into the counter and the signal line diff = 0 is monitored for correct operation.
EC 15	SEEK FORWARD CHECK A cylinder difference count is sent to the servo board. Through the D/A converter, the analog signal is propagated through the rest of the seek circuit all the way to the last stage which are the output drivers. At this point, the signal is sent back to the I/O Board for examination. A comparator is used for determining whether the signal is good or bad.
EC 16	SEEK REVERSE CHECK Similar to seek forward check (EC 15) except polarity is opposite.
EC 17	OFFSET FORWARD CHECK Similar to seek forward check (EC 15) except the signal goes through the offset circuit instead of the seek circuit.
EC 18	OFFSET REVERSE CHECK Similar to seek forward check (EC 15) except the polarity is opposite.
EC 19	SERVO DISABLE CHECK A difference count is sent to the servo board but the output drivers should both be inactive.

5.2.2 Operational Error Checking

During normal system usage and/or diagnostic self-testing a number of built-in self-tests are performed. If any error conditions are detected by the microprocessor a fault condition is indicated along with the appropriate error code display, by the fault indicators. Table 5-3 lists the tests and the applicable error codes. All error codes remain displayed until any key on the keyboard is depressed. The FAULT RESET momentary switch will allow clearing the fault condition, but will not clear the display.

5.2.3 Internal Diagnostics

The Capricorn drive has the capability of operating internal diagnostics without an external tester and without disconnecting cables from the controller. The following is a list and short description of these tests.

Seek operations are performed over all cylinders. Read/write operations are only performed on the CE cylinders and cannot access customer data tracks. These tests can be run by the use of the controls on the diagnostic keyboard located behind

Table 5-3. Operational Error Code Descriptions

ERROR CODE	DESCRIPTION
EC 21	UPSPEED DETECTION When the drive fails to come up to 3000 RPM in 15 seconds.
EC 22	POWER-FAILURE DETECTION When there is a loss of any voltage (dc).
EC 31	DRIFTED INTO GUARDBAND When the heads moved into the inner or outer guardbands other than during a rezero operation.
EC 32	REZERO TIMEOUT Takes longer than 700 MSEC to do a rezero operation.
EC 33	SEEK TIMEOUT Takes longer than 100 MSEC to do a seek operation.
EC 34	MAX. CYLINDER EXCEEDED Received a cylinder number higher than the maximum legal cylinder number.
EC 42	READ ERROR A four-block bit pattern generated by the random number generator is written on all tracks. Then during a read operation a bit-by-bit comparison of the recorded data against the pattern generated is made by the random number generator. If all four blocks contained one or more bits, a read error is displayed.
EC 43	ADDRESS MARK READ ERROR The Address Mark Read Error code is displayed when the address mark is not detected.
EC 45	SYNC ERROR The Sync Error code is displayed when the logic 1 bit that initiates the data block is not detected.
EC 46	INDEX ERROR The Index Error code is displayed when the Index Error is not detected.
EC 52	PLO ERROR When PLO error signal is low (active).
EC 53	WRITE WITH WRITE PROTECT ACTIVE Write while read only switch activated.
EC 54	WRITE WITH READ GATE ACTIVE Write gate and read gate both active.
EC 55	WRITE WITH OFFSET ACTIVE Write gate while offset active.
EC 56	WRITE WITHOUT FINE TRACK Write gate with no fine track.
EC 58	MULTI-CHIP SELECTED More than one head select chip is active.
EC 59	READ/WRITE UNSAFE A failure in the head-arm integrated circuit.
EC 61	BAD ENTRY The Bad Entry code is displayed when the keyboard selection is in a non- functional code (e.g., too many keys activated or some other type of erroneous keyboard activation).

the front panel. Refer to paragraph 3.2 for a description of the controls and indicators.

The DIAG/NORMAL switch sets the drive off-line from the controller and into the diagnostic self-test mode of operation. The keyboard functions are listed in Table 5-4. Function code descriptions are listed in Table 5-5.

The parameter table is displayed/changed by the use of the "E" examine key. All Values (except for E 01) are displayed as decimal values and can be altered by keying in a new 4-digit decimal value and observing the limits for the particular drive. Examine function descriptions are listed in Table 5-6.

Table 5-4. Keyboard Functions

Key	Function
A	Single Cycle Rezero-- Each time the button is depressed a rezero operation is performed.
B	Break-- Depressing the button causes interruption of the test routine running.
C	Continue-- Depressing the button allows starting a set default series of tests or allows starting a test after selecting test with the function key.
D	Delete-- Clears display of error codes or parameter entries.
E	Examine-- Allows displaying/changing parameters from the parameter table.
F	Function-- Allows selection of test to run.

Table 5-5. Function Code Description

Function Code	Description
None	SINGLE REZERO Single cycle rezero -- each time the button (Key A) is depressed, a rezero operation is performed.
F 11	RANDOM SEEK Seeking randomly across the data area.
F 12	SEQUENTIAL FORWARD AND REVERSE SEEKS Seeking sequentially with programmable steps (increments). (8-track)
F 13	ALTERNATE Seeking back and forth between two given cylinders. (0 and 1033)
F 14	WRITE ONLY Performs the write operation only. (1033)
F 15	READ ONLY Performs the read operation only. (1033)
F 16	READ/WRITE Performs read after write. (1033)
F 17	COMBINATION A combination of read/write and seek between two alternate CE tracks. (1024 and 1033)
F 18	ERROR LOGGING Displays up to 31 stored EC error codes.

Table 5-6. Examine Function Descriptions

Examine Code	Description
E 01	Examine run-condition flagword Default Value: 0000 Digit 0 : 1 = Stop on error Digit 1 : 1 = Suppress display of error codes Digit 2 : 1 = Display cylinder number Digit 3 : 1 = Display seek time (ms) DIGIT 3 2 1 0 DS4DS3DS2DS1
E 02	Examine lower cylinder limit
E 03	Examine upper cylinder limit
E 04	Examine lower cylinder limit
E 05	Examine upper cylinder limit
E 06	Examine cylinder increment (used for sequential seek test F12)
E 07	Examine upper and lower head limit digit 0 and 1 displays lower head limit digit 2 and 3 displays upper head limit (used for F14 through F17)
E 08	Examine seek interval time (time is displayed in ms)

For example, to change the lower cylinder limit to 0025:

1. Press E 02.
2. Press "C".
3. Press 0025 (always include leading zeros).
4. (a) Press "C" to enter new limit into memory.
(b) or press "D" to preclude limit change.
5. Press "C" again to continue with previous function.
6. Or, enter a new function code.
7. To return to the default mode - toggle diagnostic switch to NORMAL or press CB1 to off.

5.3 ADJUSTMENTS AND ALIGNMENTS

The checks described in the following paragraphs are included in this manual as information only, but they may be of use when troubleshooting portions of the disk drive. Adjustments must be performed by qualified field service personnel. No special tools or test equipment are required for the performance of these procedures.

5.3.1 Brake Adjustment

The following procedure should be performed for adjusting the brake.

CAUTION

Erroneous wiring connections can damage the equipment. Observe and record exact plug-to-plug connections before disconnecting connectors. Use care to install wires to the correct pins and mating connectors, as recorded.

1. Ascertain that circuit breaker CB1 (Figure 2-9) is in Off position.
2. Remove top cover (paragraph 5.4.2).
3. Remove optional dual-port PCBA (paragraph 5.4.4).
4. Disconnect drive motor connector P8 and linear motor connector P3 at power supply (paragraph 5.4.6).

CAUTION

Connecting pin A1J9-6 and A1J9-7 on I/O PCBA 3309783-01 to dc ground (A1J9-2, 3, or 5) will pull in (disengage) the brake and, connecting pin A1J9-6 to dc ground only, will keep the brake disengaged after initial pull-in.

5. On I/O PCBA A1 (3309783-01) set LOCAL/REMOTE switch S5 to LOCAL position (Up position). Power cord should be connected to an appropriate line source at this time.

CAUTION

Before performing step 6, place the Capricorn drive on a work bench or any other solid and level surface.

NOTE

Before performing step 6, turn the drive over on one side so the OCP is located near the bottom. With the drive on its side, the brake components are easier to adjust.

6. Remove belt cover screws and belt cover. Set circuit breaker CB1 to On position; observe that brake pad pulls away from HDA spindle. Connect A1J9-6 to dc ground; after not less than 15 seconds, ascertain that gap still exists between brake pad and HDA spindle pulley.
7. If step 6 is satisfied, disconnect grounding connection from A1J9-6 and continue to step 22.

8. If step 6 is not satisfied (i.e., no gap exists between spindle pulley and brake pad) turn breaker CB1 to Off position, connect A1J9-6 and A1J9-7 to dc ground and continue to step 9.

NOTE

If the brake hold-down screws are loosened too much during the next step, extra effort will be required during step 11 to help the pick-up coil pull in the brake.

9. Loosen brake hold-down screws (Figure 5-1) by approximately 1/4 turn. Remove ground contact assembly by loosening two screws that hold assembly to brake body and slide assembly toward spindle.

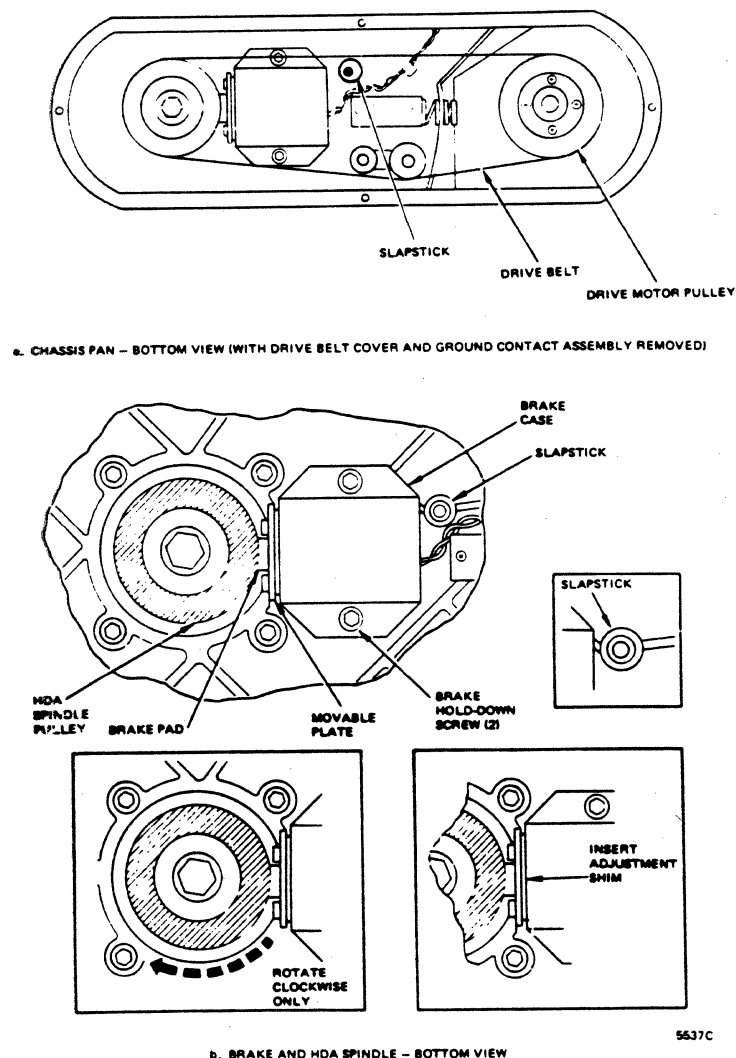


Figure 5-1. Brake Adjustment Detail

NOTE

The next step requires a metal shim of approximately 1-1/4 inches square and 0.003-inch thick.

10. Insert metal shim between brake and movable plate to a distance of 1-1/8 inches (nominal), and hold shim in this position.

CAUTION

If it becomes necessary to rotate the pulley on the HDA during the following steps, make sure the pulley is rotated only in the clockwise direction as seen from the bottom of the HDA (Figure 5-1).

CAUTION

Be prepared to perform steps 11 and 12 within 5 minutes to prevent possible damage to the coil.

NOTE

During step 11 only, use heavy screwdriver as a lever placed against HDA rib and backside of linear brake to push brake toward spindle pulley.

CAUTION

During step 11, avoid pinching the brake leads between screwdriver and brake case.

11. Set circuit breaker CB1 to On position; and push brake toward spindle pulley until plate retracts and holds shim in place.
12. Loosen brake hold-down screws and push brake case by hand towards pulley until entire arc of brake pad contacts the pulley; tighten Allen-head screws while maintaining pressure on brake case (Figure 5-1).
13. Ascertain that belt does not contact brake case.
14. Set circuit breaker to Off position.
15. Remove shim stock.

NOTE

After completion of step 16, wait not less than 15 seconds before performing step 17.

16. Set circuit breaker CB1 to On position to disengage brake; remove dc ground connection from A1J9-7.

CAUTION

In steps 17 and 19, make sure to rotate the HDA only in the clockwise direction as seen from the bottom of the HDA (Figure 5-1). Rotating the HDA in the wrong direction can damage the HDA.

17. Try to rotate HDA pulley in a clockwise direction as seen from the bottom of the HDA (Figure 5-1); pulley should rotate freely.

NOTE

Performance of the next step causes the brake to engage, provided the circuit breaker has been in the On position for not less than 15 seconds.

18. Remove dc ground connection from pin A1J9-6 of PCBA A1.

CAUTION

In the next step, make sure to rotate the HDA only in the clockwise direction as seen from the bottom of the HDA (Figure 5-1). Rotating the HDA in the wrong direction can damage the HDA.

19. Try to rotate HDA in the clockwise direction (Figure 5-1) as seen from the bottom of the HDA; observe that HDA pulley is difficult to rotate.
20. Set circuit breaker CB1 to Off position.
21. Install ground contact assembly with contact centered on the spindle pulley bolt ball.
22. Return drive to normal upright position.
23. Reconnect drive motor connector P8 and linear motor connector P3.
24. Brake adjustment is complete.
25. Reinstall dual-port PCBA (paragraph 5.4.4).
26. Reinstall top cover (paragraph 5.4.2).

5.3.2 Logic Power Supply Adjustment

Logic power should be measured at the input of the I/O Control PCBA (A1) and adjusted at the power supply regulator PCBA (A6). Use of a digital voltmeter (Hewlett Packard 34701 A or equivalent) is recommended for performing this adjustment. The following procedure should be used to adjust the logic power supply.

1. Remove top cover (paragraph 5.4.2).
2. Power up drive (paragraph 3.3.1).
3. Connect digital voltmeter (DVM) between +5V at A1J9-1 and ground at A1J9-2 (Figure 5-2).

WARNING

Extreme care must be taken when working on the power supply. The ac power cord to the fan carries dangerous high-voltage current. Use an insulated adjusting tool (i.e., tweaker) to perform adjustment.

NOTE

In the next step, use one of the holes in the safety shield directly over variable resistor A6R3 to gain access to A6R3 with the tweaker.

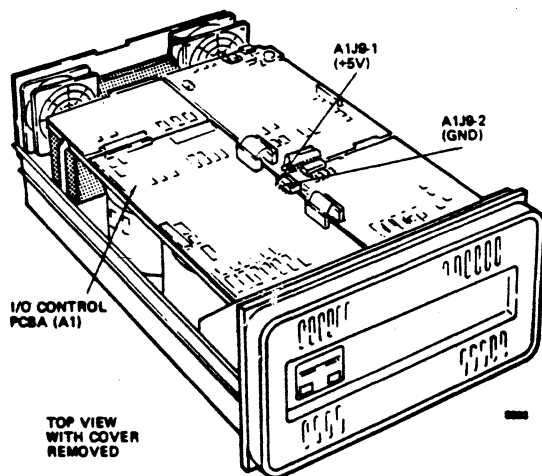


Figure 5-2. Measurement Location for +5V Logic Power Check

4. Adjust potentiometer A6R3 (Figure 5-3) until DVM measures $+5.1V \pm 0.1V$.
5. Disconnect DVM between A1J9-1 and A1J9-2.
6. Power down drive (paragraph 3.3.2).
7. Replace top cover (paragraph 5.4.2).

5.3.3 Servo Adjustment

Servo PLO circuits are factory adjusted. Since the need for adjustment is to compensate for circuit parameter variations, no additional adjustments should be necessary. However, the following procedures should be used when removing and replacing the Servo PCBA (A3).

1. Power up drive (paragraph 3.3.1).
2. Set DIAG/NORMAL switch (Figure 3-1) to DIAG position.
3. Connect oscilloscope (Tektronix 465 or equivalent) to A3TP7 and set dc offset of signal to $0 \pm 0.01 V_{dc}$ by adjusting variable capacitor A3C33.
4. Rezero drive (Function Key A).

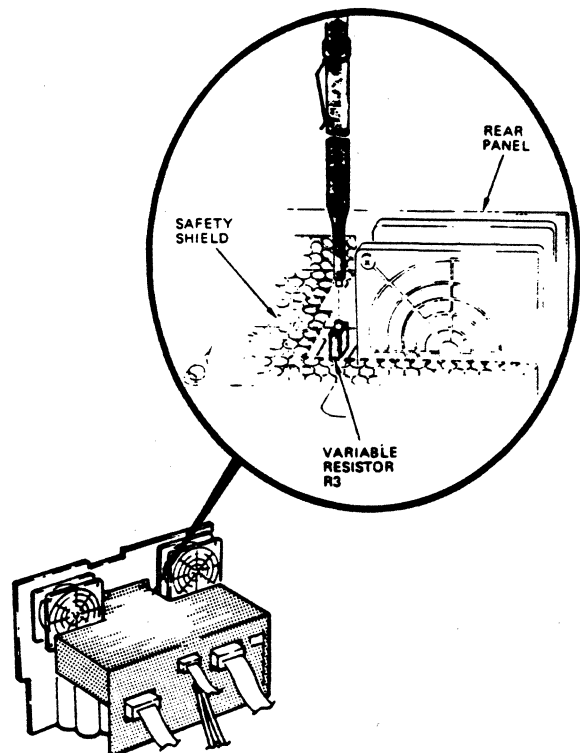


Figure 5-3. Adjustment Location for +5V Power Supply Regulator

5. Connect oscilloscope to A3TP2 and set d-c offset of signal to 0 ± 0.1 Vdc by adjusting potentiometer A3R34.
6. Set DIAG/NORMAL switch (Figure 3-1) to NORMAL position.
7. Power down drive (paragraph 3.3.2).

5.3.4 Servo Seek Time Adjustment

The servo seek timing adjustment should be used to accommodate variations in linear motor parameters. Seek timing is factory adjusted. However, the following procedures should be used when removing and replacing the Servo PCBA (A3).

1. Power up drive (paragraph 3.3.1).
2. Set DIAG/NORMAL switch (Figure 3-1) to DIAG position.
3. Execute diagnostic command F13 (i.e., seek between track 0 and track 1033, the last CE track).
4. Connect oscilloscope (Tektronix 465 or equivalent) to A1TP1 and trigger on falling edge (+5V= on cylinder, or 0 = seeking).
5. Adjust variable resistor A3R25 to set timing between falling edge and rising edge to 57 milliseconds ± 2 milliseconds for a Model 330 and to 48 ± 2 milliseconds for Model 165. (See Figure 5-4).

6. Rezero drive (Function Key A).

7. Power down drive (paragraph 3.3.2).

5.3.5 Read/Write Adjustments

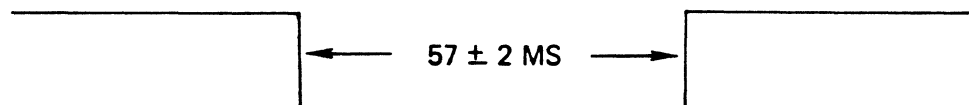
The read/write adjustments consist of four separate procedures. Performance of all four procedures is required when the Read/Write PCBA (A2) is removed and replaced. Use of an oscilloscope (Tektronix 465 or equivalent) is recommended for performing these adjustments.

5.3.5.1 Phase Lock Loop Voltage Adjustment

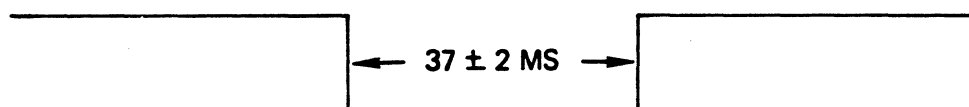
The phase lock loop (PLL) voltage adjustment should be used to accommodate variations in spindle speed and servo PLL frequency. The procedure should be performed as follows.

1. Remove top cover (paragraph 5.4.2).
2. Power up drive (paragraph 3.3.1).
3. Using oscilloscope, trigger time base on Index (A1TP7) and set sensitivity to 2 ms/div so one spindle revolution is displayed on oscilloscope.
4. At oscilloscope, set vertical amplifier sensitivity to 100 mV/div and establish ground at center line of display; enable 20 MHz bandwidth with channel d-c coupled; and monitor PLL voltage at A2TP5.

a. MODEL 330



b. MODEL 165



5699

Figure 5-4. Seek Timing Adjustment

NOTE

It may be necessary to reduce the vertical sensitivity initially until the error voltage is sufficiently close to 0 V. Also, the error voltage will drift from this setting with time and temperature.

5. Adjust variable capacitor A2C1 until average voltage error is zero on one revolution (16.67 ms). Maximum excursion about this average should be no more than 40 mV. A typical adjusted error voltage waveform is shown in Figure 5-5.
6. Set DIAG/NORMAL switch (Figure 3-1) to NORMAL position.
7. Proceed to next adjustment.

5.3.5.2 VFO Window Adjustment/Check

Window centering is factory adjusted. Since the need for adjustment is to compensate for circuit parameter variations, no additional adjustments should be necessary. However, the following procedures should be used when removing and replacing the Read/Write PCBA (A2).

NOTE

Step 1 defines the threshold for ECL (-1.3V) at centerline and establishes the 50 percent point for timing measurements.

1. At oscilloscope, set vertical amplifier sensitivities of channels 1 and 2 to 500 mV/div and establish ground for channel 1 at 2.6 divisions above display centerline.

2. At oscilloscope, dc couple both amplifiers; monitor 2F VFO clock (A2TP4) with channel 1 and input clock (A2TP2) with channel 2; and adjust offset of channel 2 so signals do not overlap in alternate mode.
3. Set time base at 5 ns/div and trigger on positive going edge of channel 1 (2F VFO at A2TP4); and establish time mark at 50 percent point of falling edge of 2F VFO.

NOTE

In the next step, it may be necessary to retrigger the scope so that the switching time will occur in the displayed window.

4. Adjust variable resistor A2R28 until crossover of input clock A2TP2 coincides with -1.3V transition point of A2TP4 as shown in Figure 5-6.
5. Switching time of input clock (A2TP2) should fall within 1 nanosecond of mark with no more than 1 nanosecond of jitter. Refer to Figure 5-6 for example of properly centered VFO.

NOTE

The switching time of the input clock is defined as the average center of the crossover created by the positive- and negative-going edges. Jitter is defined as the width of the crossover at the switching time.

6. Proceed to next adjustment.

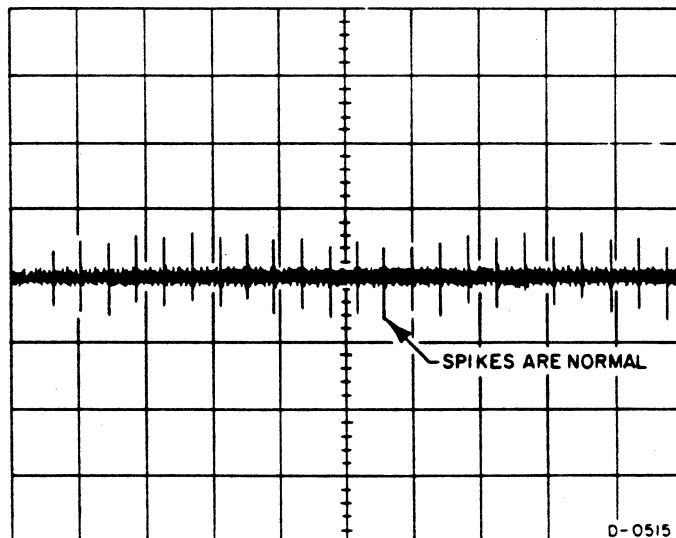


Figure 5-5. Error Voltage Waveform

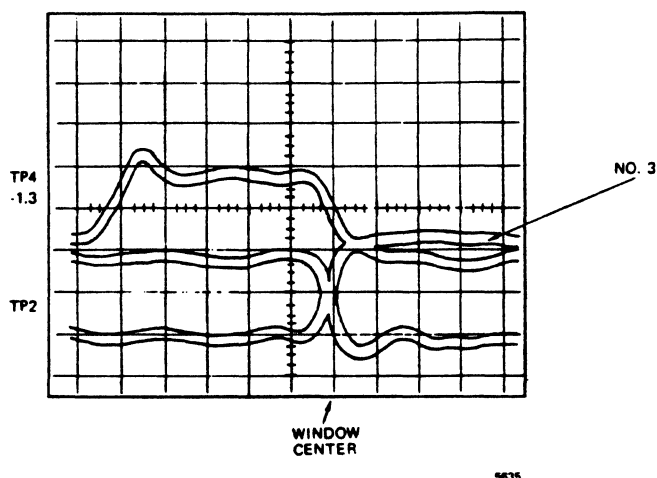


Figure 5-6. Example of Properly Centered VFO

5.3.5.3 Data Jitter/Peak Shift Check

Data jitter and peak shift are measures of the quality for the heads, disks, and read/write channel. In some cases, this check can be useful in identifying a defective Read/Write PCBA (A2) or head disk assembly.

1. Set DIAG/NORMAL switch (Figure 3-1) to DIAG position.

NOTE

Step 2 defines the threshold for ECL (-1.3V) at centerline and establishes the 50 percent point for timing measurements.

2. At oscilloscope, set vertical amplifier sensitivities of channels 1 and 2 to 500 mV/div and establish ground for channel 1 at 2.6 divisions above display centerline.
3. At oscilloscope, dc couple both amplifiers; monitor 2F VFO clock (A2TP4) with channel 1 and input clock (A2TP2) with channel 2; and adjust offset of channel 2 so signals do not overlap in alternate mode.
4. Execute diagnostic routine F15 (i.e., read only - CE tracks).
5. Externally trigger time base on falling edge of READ GATE (A2TP1) in ac coupled mode; delay trigger on rising edge of 2F VFO clock (A2TP4, channel 1) with delay set at 3 or 4 divisions; set main time base at about 50 microseconds per division; set delay time at 10 nanoseconds per division; and observe displayed waveform.

6. Display should resemble Figure 5-6, except that crossover of input clock A2TP2 should be smeared (i.e., jitter). If displayed waveform is correct, skip to step 8. If display indication is incorrect, continue with step 7.

NOTE

In step 7, the persistence of the scope trace is low and requires the use of a scope hood.

7. Repeat step 5 and observe displayed waveform. Crossover of input clock A2TP2 should be contained within a region bounded by plus or minus 10 nanoseconds of mark.
8. Proceed to Read/Write performance check.

5.3.5.4 Read/Write Performance Check

The read/write performance check should be used to check the operational performance of the Read/Write PCBA (A2).

1. Set DIAG/NORMAL switch (Figure 3-1) to DIAG position.
2. Execute diagnostic command F17 (i.e., read, write, and Seek on CE tracks); test should be run for 5- to 10-minutes duration without error.
3. Break diagnostic routing (Function Key B).
4. Set DIAG/NORMAL switch (Figure 3-1) to NORMAL position.
5. Power down drive (paragraph 3.3.2).

5.4 REMOVAL AND REPLACEMENT PROCEDURES

The following paragraphs explain the removal and replacement procedures for the major Capricorn subassemblies. Refer to Figure 5-7 to locate the relative position of each

subassembly within the drive. Be sure to read each procedure before attempting any removal or replacement.

5.4.1 Optional Slide Rails

Refer to paragraph 2.3.1.2 for slide rail removal and replacement procedures.

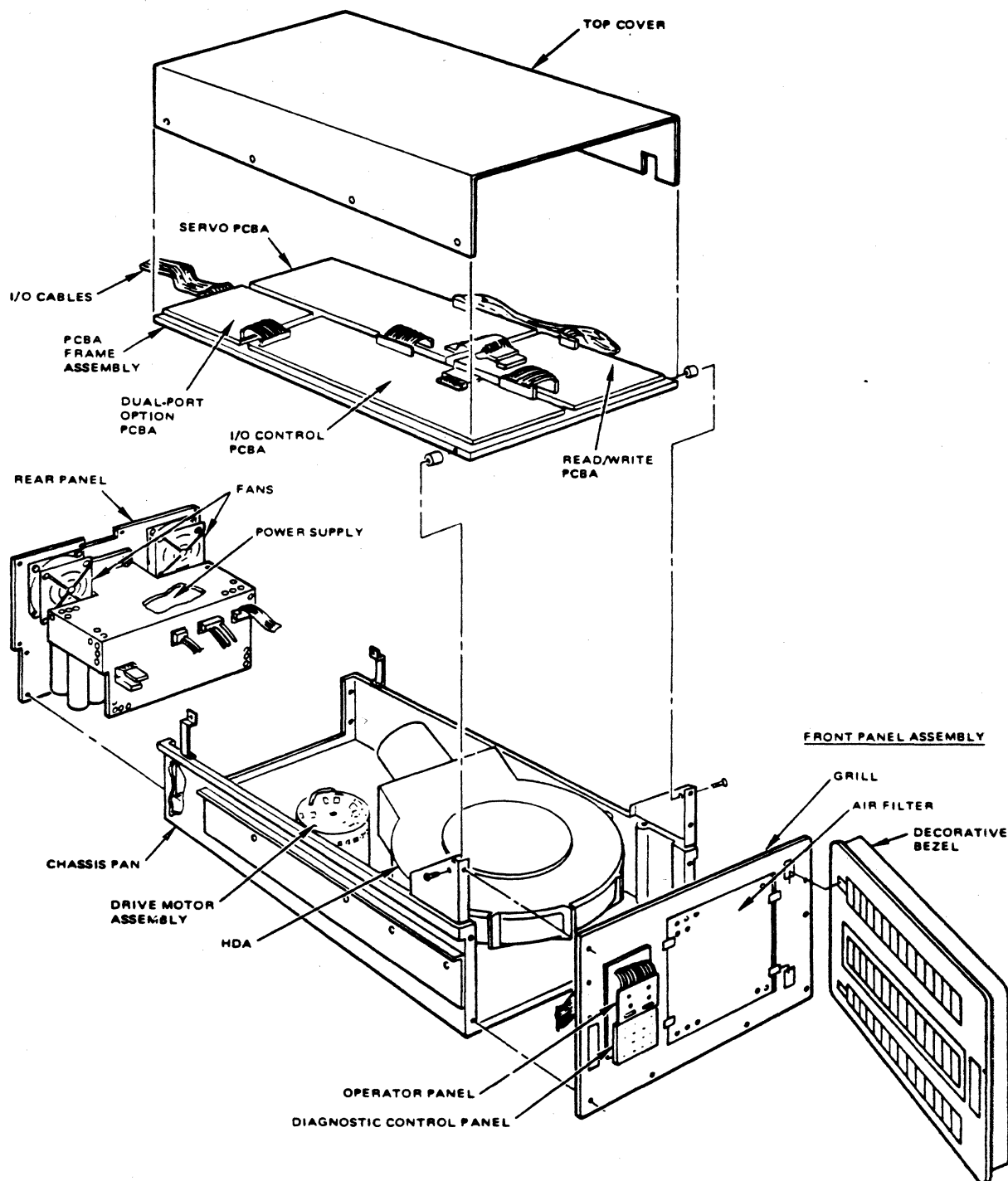


Figure 5-7. Capricorn Subassembly Locations

5526

5.4.2 Top Cover

The top cover, as shown in Figure 5-8, is held in place by fifteen panhead screws. To remove the top cover;

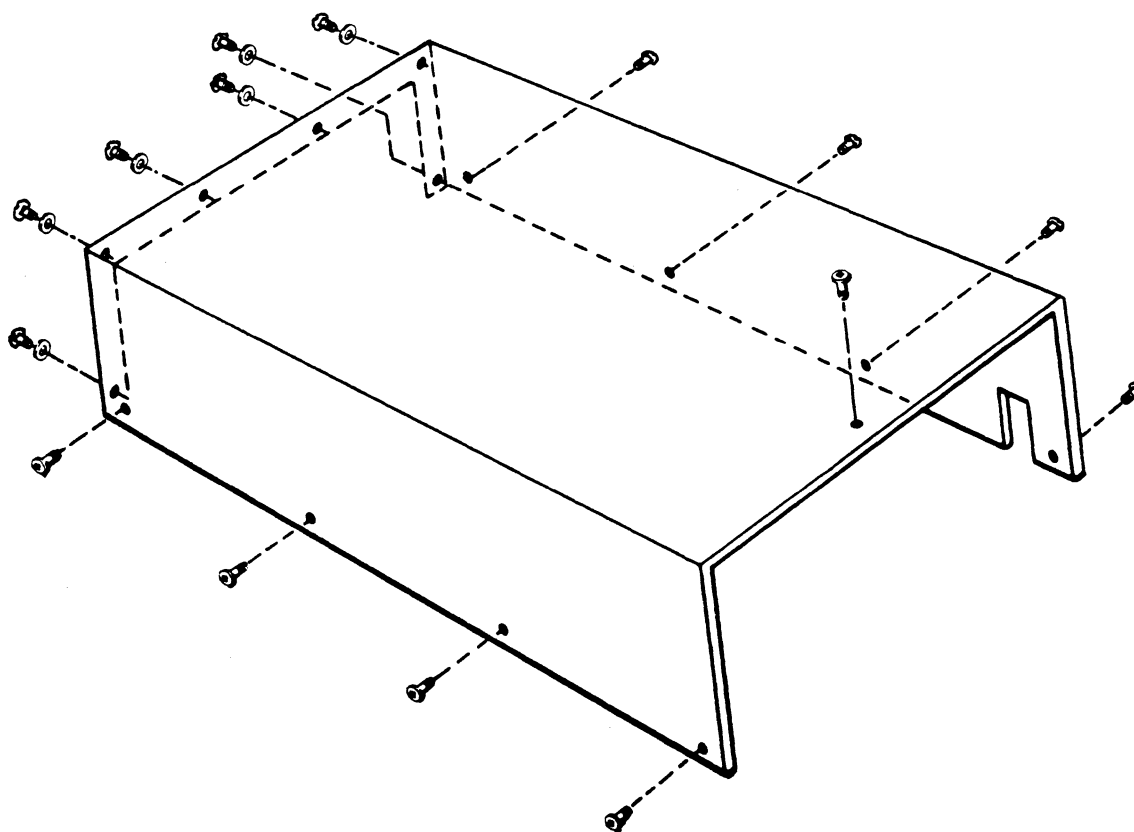
1. Remove four screws along each right and left lower edge of top cover.
2. Remove single screw from top front edge of top cover.
3. Remove six screws with washers from lip at rear of the top cover.
4. Gently lift top cover from the drive.

To reinstall the top cover, perform the above steps in reverse order.

5.4.3 Front Panel Assembly

The front panel assembly comprises of a decorative bezel, a grill, and an air filter. Perform the following steps to remove the front panel assembly:

1. Remove top cover as described in paragraph 5.4.2.
2. Open bezel door and remove air filter from its four clips.



5527A

Figure 5-8. Top Cover

3. Remove bezel by lifting and turning hinge pins as shown in Figure 5-9.
4. Remove diagnostic cable clamp (not shown).
5. Disconnect diagnostic cable (Figure 5-9) from Read/Write PCBA.
6. Remove ten Phillips screws that hold grill to frame assembly, as shown in Figure 5-9.

To reinstall the front panel assembly, perform the above steps in reverse order.

5.4.4 Printed Circuit Boards

The Servo, Read/write, I/O control and optional Dual-port PCBAs are field-replaceable. The locations of these PCBAs with ribbon-cable and power intraconnections are shown in Figure 5-10.

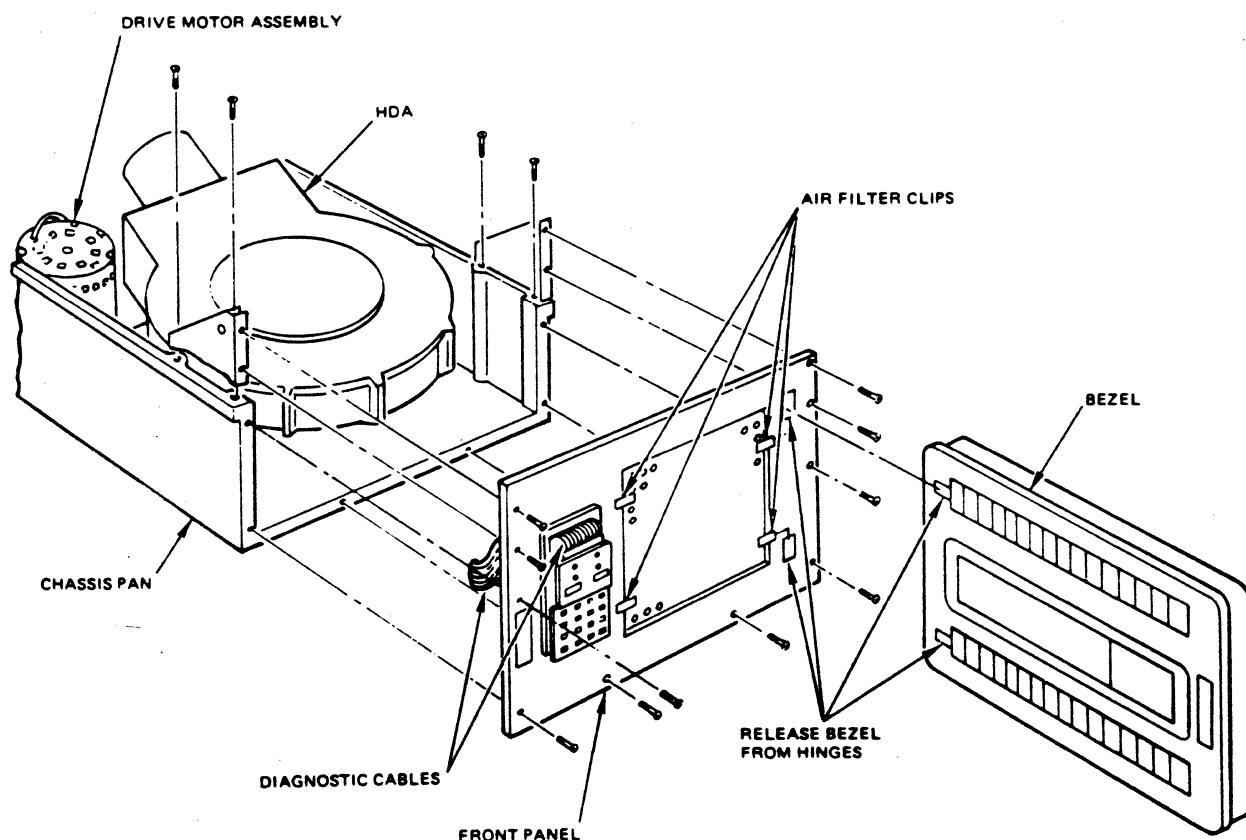
To remove any PCBA, perform the following steps:

1. Remove top cover as described in paragraph 5.4.2.
2. Disconnect appropriate ribbon cables (Figure 5-10).
3. Carefully lift PCBA off its fastening pegs.
4. Detach power interconnection (A1P9, A2P3, or A3P9, as applicable) from the topside of the PCBA (see Figure 5-10 for location of the power interconnect).

To reinstall a PCBA, perform the above steps in reverse order.

5.4.5 PCBA Frame Assembly

Perform the following steps to remove the PCBA frame assembly:



5528

Figure 5-9. Front Assembly

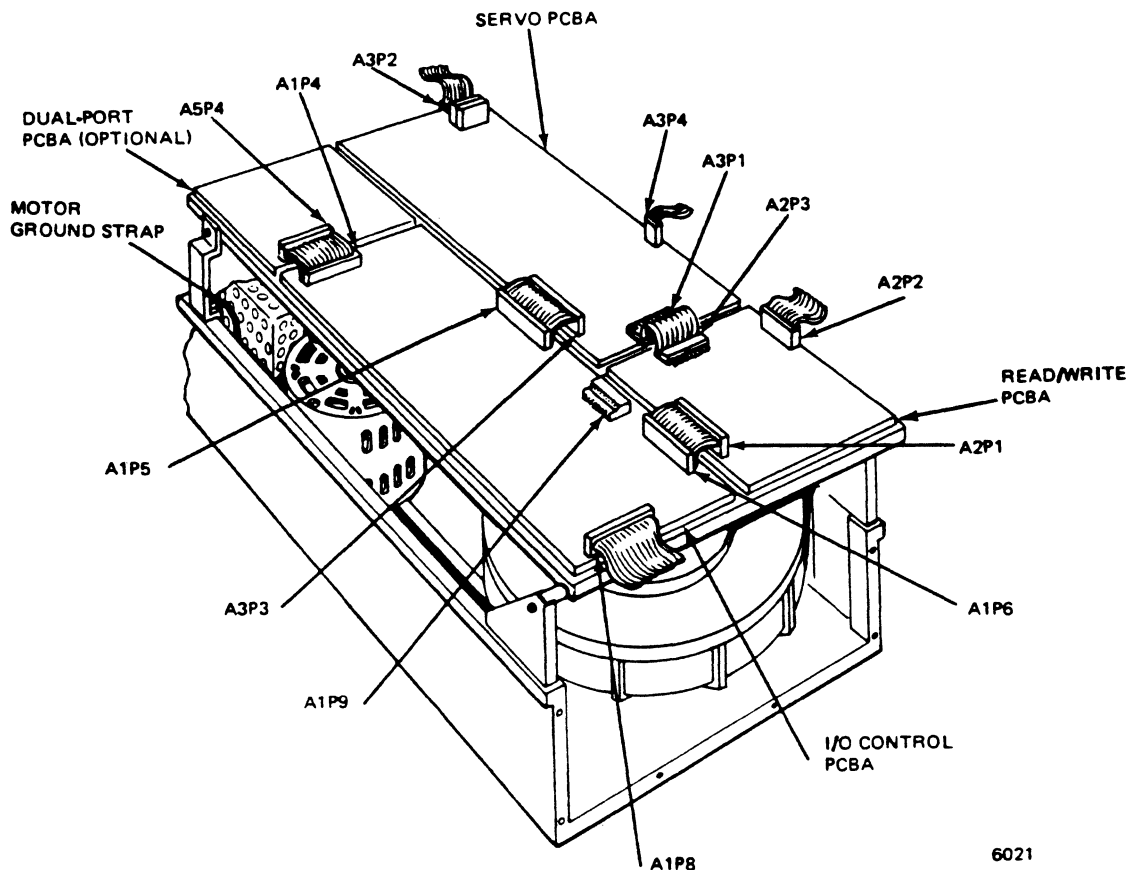


Figure 5-10. PCBAs with Ribbon-Cable and Power Intraconnections

1. Remove top cover as described in paragraph 5.4.2.
2. Disconnect ribbon cable connectors A1P8, A2P2, and A3P4 as shown in Figure 5-11.
3. Disconnect power cable connector A6P4 and A6P5 at power supply; disconnect ground from connector A1J10.
4. Loosen and remove four screws that attach PCBA frame to chassis pan extensions, as shown in Figure 5-11. Lift frame out of drive.
5. Replace top cover as described in paragraph 5.4.2.

To reinstall the PCBA frame assembly, position the frame assembly properly on the chassis pan; place the spacers between the assembly and both mounting brackets with the counter-sunk side towards the mounting bracket; and replace the screws.

CAUTION

While reinstalling the PCBA frame assembly, care must be taken to prevent the power distribution cable from being pinched between the PCBA frame assembly and the top of the HDA.

5.4.6 Power Supply

Refer to Figure 5-12 and perform the following steps to remove power supply:

1. Remove top cover as described in paragraph 5.4.2.
2. Remove six Phillips screws at outer edges of rear panel, as shown at top of Figure 5-12.
3. Disconnect ground strap from I/O control PCBA and from optional dual-port PCBA.

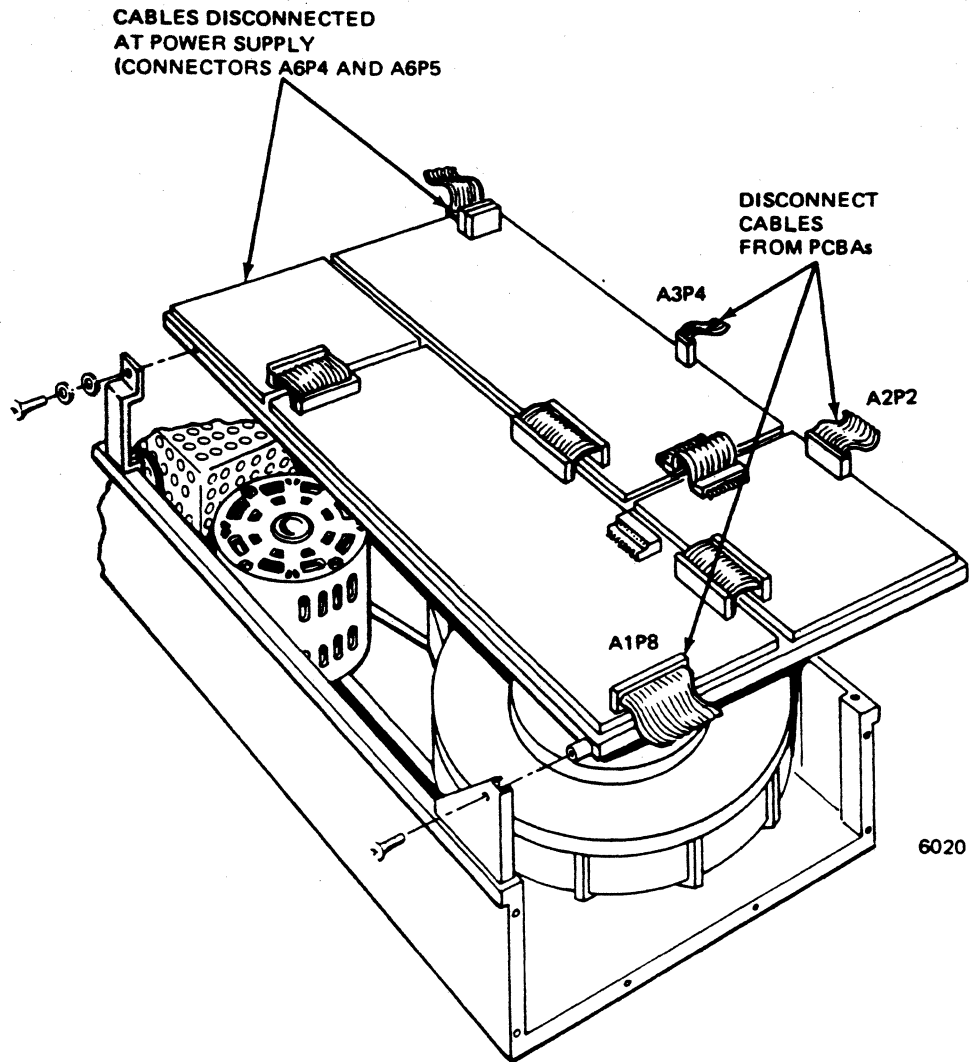


Figure 5-11. Frame Assembly Removal

4. Disconnect ground strap from upper right corner of HDA by removing strap-ring-lug screw (hex head).
5. Carefully pull power supply away from chassis pan until cable connectors are accessible.
6. Detach five cables from power supply connectors J3, J4, J5, J7, and J8, as shown in Figure 5-12.
7. Pull power supply away from drive.

CAUTION

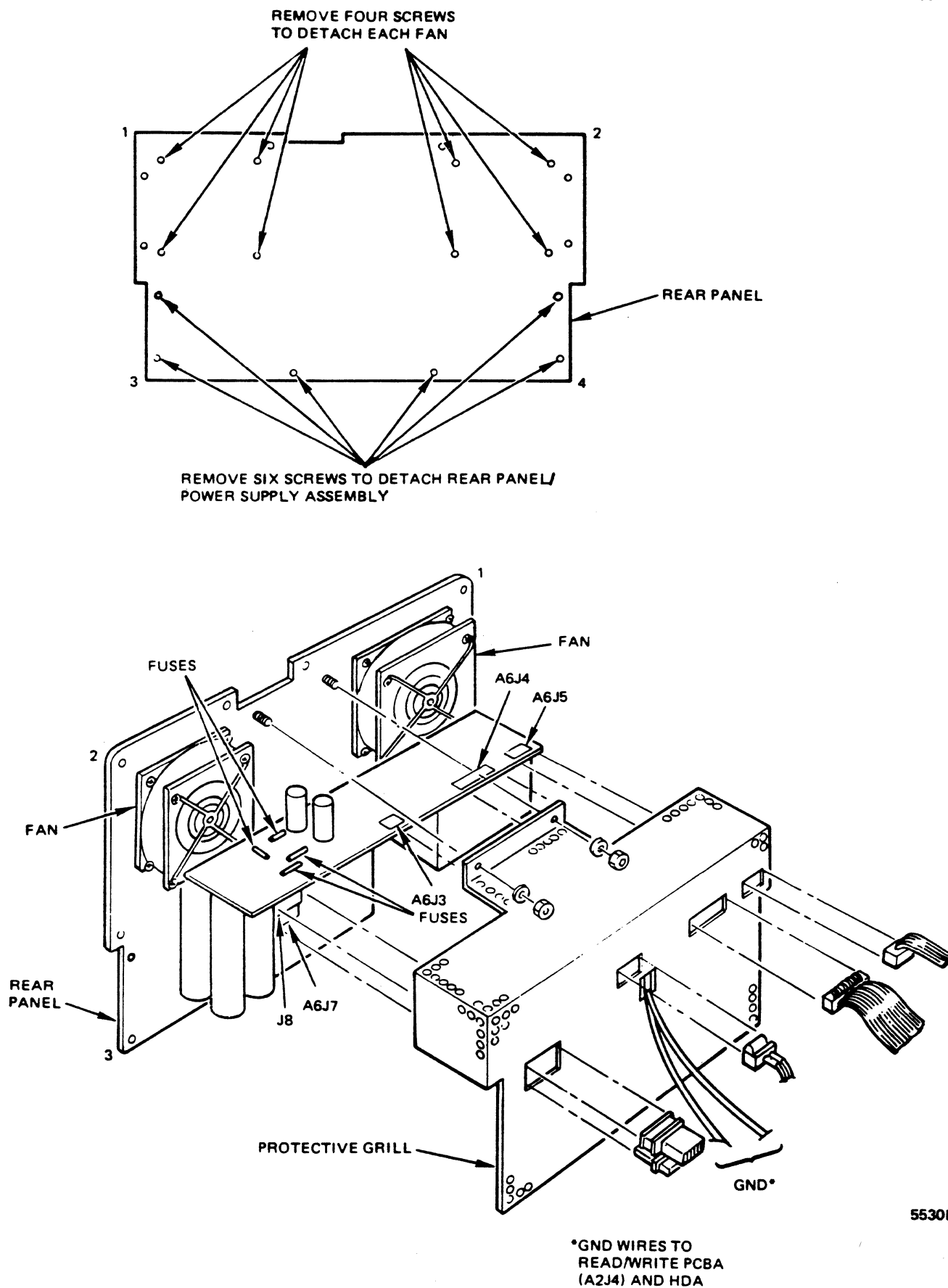
Ascertain that the power distribution cable is not pinched between the PCBA frame assembly and the top of the HDA.

To reinstall the power supply, perform the above steps in reverse order.

5.4.7 Fans

To remove either of the two ac fans perform the following steps:

1. Remove top cover as described in paragraph 5.4.2.
2. Remove power supply assembly as described in paragraph 5.4.6. (The fans are attached to the rear panel of the power supply assembly.)
3. Remove two nuts and one screw that hold protective grill onto power supply assembly, as shown on right in Figure 5-12. Removing grill also makes fuses accessible.
4. Remove four screws that hold each fan onto rear panel, as shown on left in Figure 5-12.



55308

Figure 5-12. Power Supply Assembly

5. Detach positive and ground ac wires from quick disconnects on fan.
6. Lift fan away from power supply.

To install the fans, perform the above steps in reverse order.

5.4.8 Drive Motor

Perform the following steps to remove the drive motor.

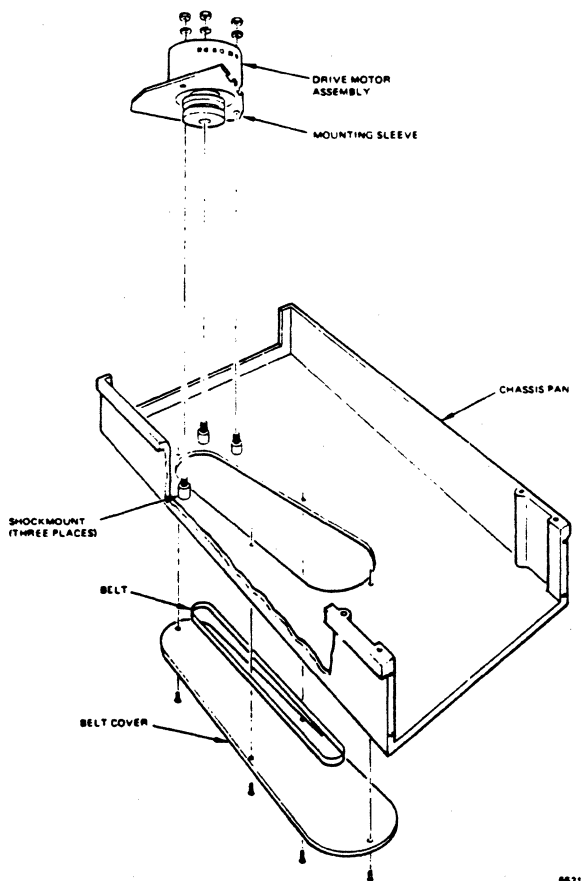
1. Remove top cover as described in paragraph 5.4.2.
2. Remove PCBA frame assembly as described in paragraph 5.4.5.
3. Remove power supply as described in paragraph 5.4.6.
4. Remove attaching screw, left rear PCBA frame bracket, and motor ground strap (Figure 5-10) from the chassis pan.

5. Remove belt cover from bottom side of drive by removing four attaching screws (Figure 5-13).
6. Depress spring into holder and insert 1/8-inch diameter pin or Phillips type screw driver (Xcelite X-100) through both holes in cylindrical springholder (Figure 5-14).

CAUTION

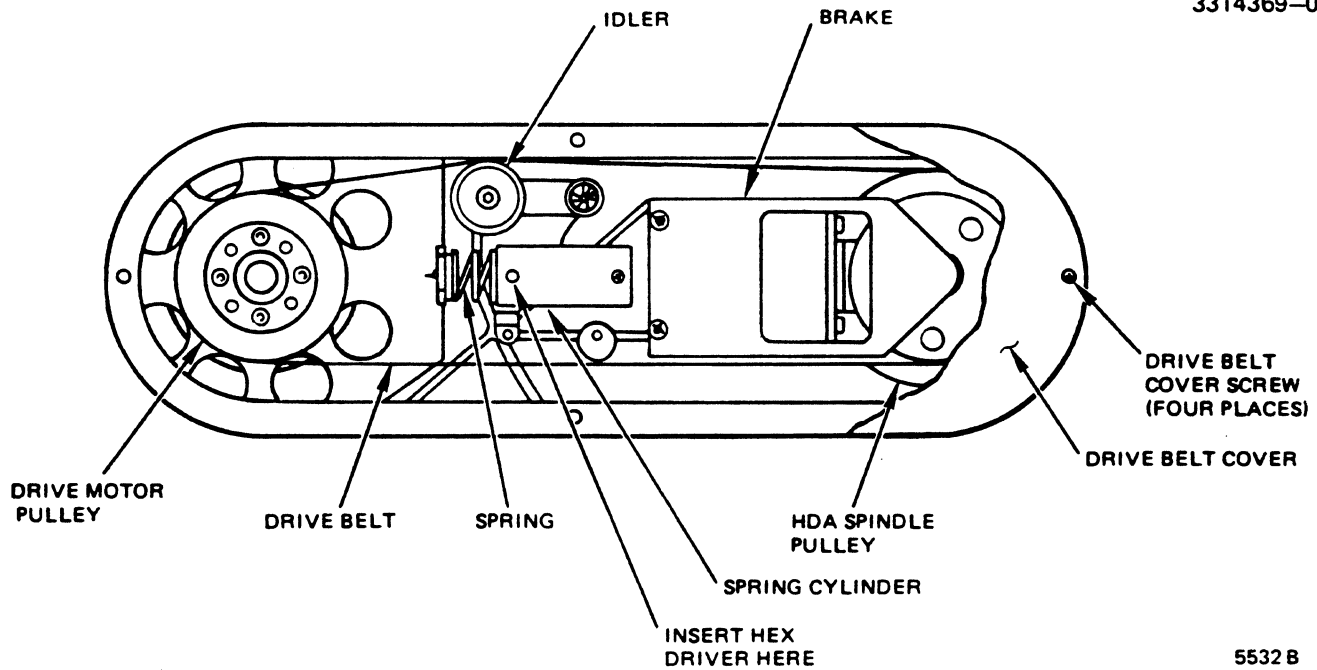
Ascertain that the pin or screw driver will remain in its position during the following steps to prevent the spring from flying out of its holder.

7. Remove three nuts which attach motor assembly to shock-mounts in chassis pan.
8. While pushing motor assembly towards HDA and idler against spring, slide belt off motor-pulley.
9. Remove drive belt.



5631A

Figure 5-13. Drive Motor



5532 B

Figure 5-14. Chassis Pan-Bottom View

10. Remove motor assembly.

Perform the following steps to reinstall the drive motor (Figure 5-13).

1. Reinstall motor assembly on shock-mounts without tightening three nuts and push assembly towards contained spring for correct seating of spring.
2. Wrap drive belt around HDA spindle-pulley; push motor assembly towards HDA and idler against spring; and slide drive belt onto motor pulley.
3. Remove pin or screw driver from spring holder.
4. With belt centered on motor-pulley, push motor assembly away from HDA until outside diameter of idler pulley is in line with edge of chassis pan opening.
5. Tighten three mounting nuts.
6. Reinstall belt cover and four attaching screws.
7. Reinstall left rear PCBA mounting bracket, motor ground strap, and attaching screw.
8. Reinstall power supply (paragraph 5.4.6).
9. Reinstall PCBA frame assembly (paragraph 5.4.5).

10. Reinstall top cover (paragraph 5.4.2).

5.4.9 HDA

To remove the HDA, refer to Figure 5-15 and perform the following steps.

1. Remove top cover as described in paragraph 5.4.2.
2. Remove frame assembly as described in paragraph 5.4.5.
3. Remove drive belt as described in paragraph 5.4.8.
4. In order to relieve tension on spring, loosen three bolts that fasten drive motor to chassis pan.
5. Loosen and remove three nuts that fasten HDA to chassis.
6. Lift HDA away from chassis. Place HDA **UPSIDE DOWN** on a stable work surface until it is ready to be reinstalled.

CAUTION

In order to prevent damage to the equipment, never set an HDA on its spindle. The correct attitude of the removed HDA is upside down on a sturdy, flat surface. Care should be taken to prevent accidental rotation of the spindle.

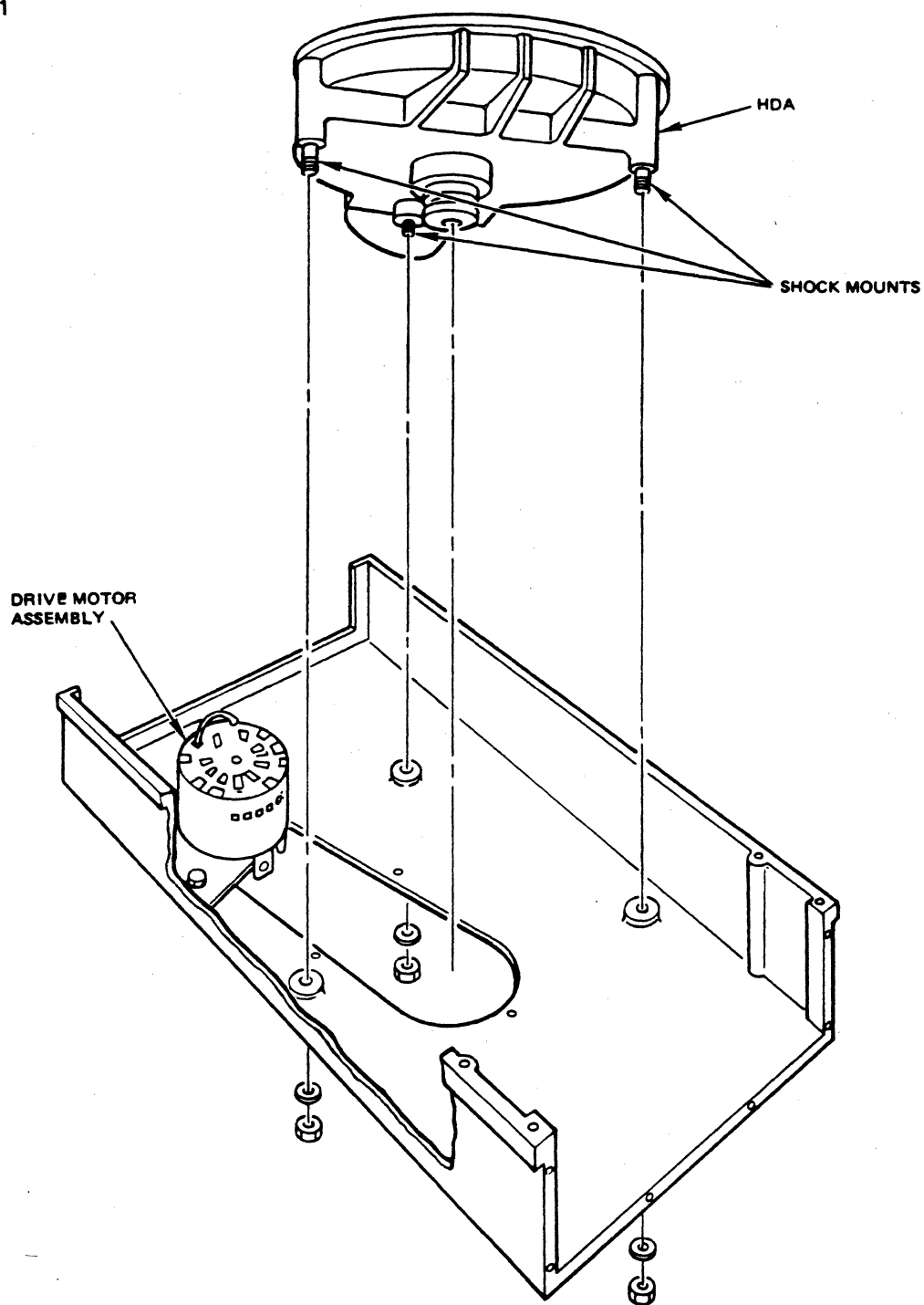


Figure 5-15. Head Disk Assembly (HDA)

8833

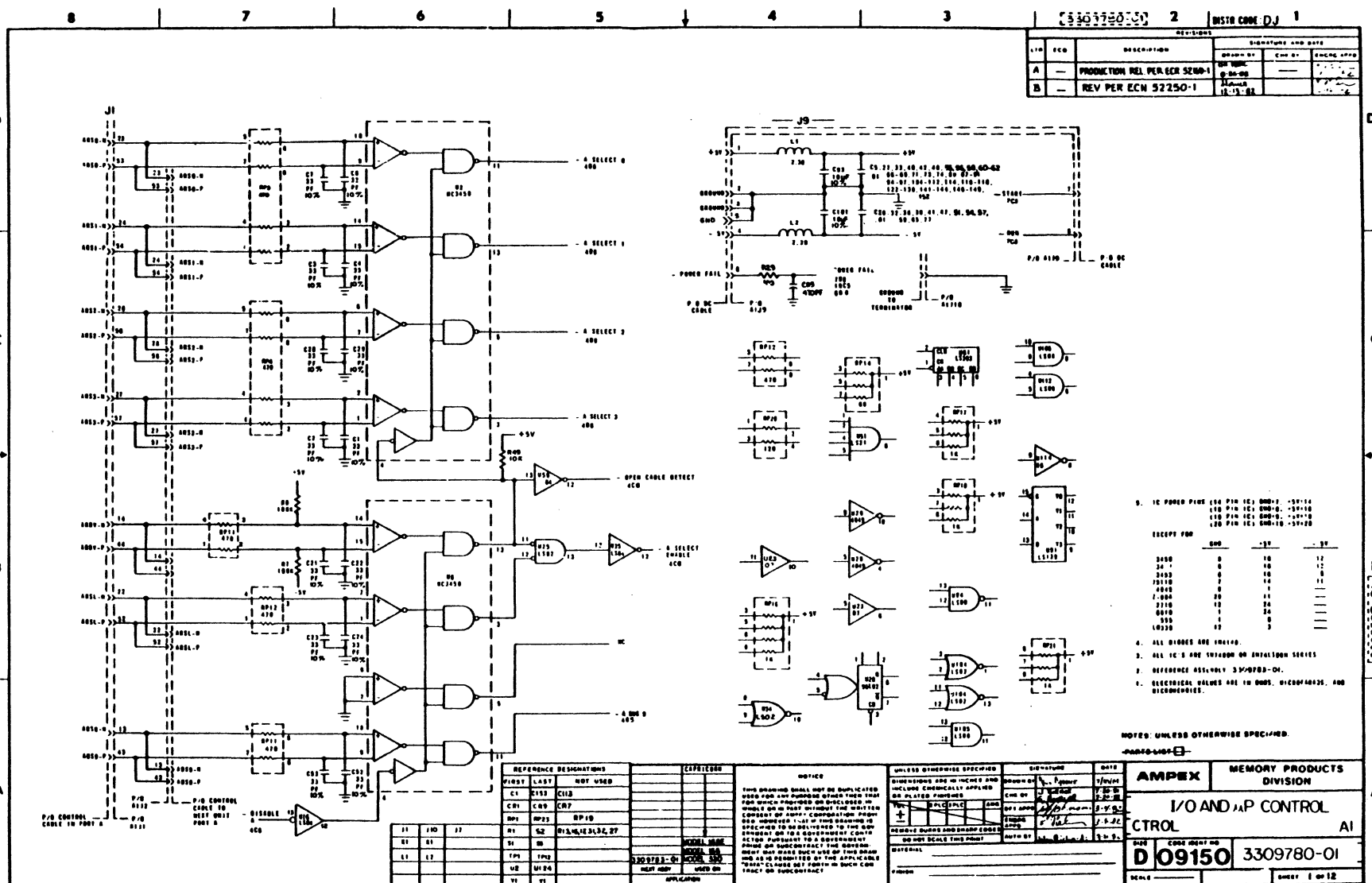
To reinstall the HDA, refer to Figure 5-15 and perform the following steps:

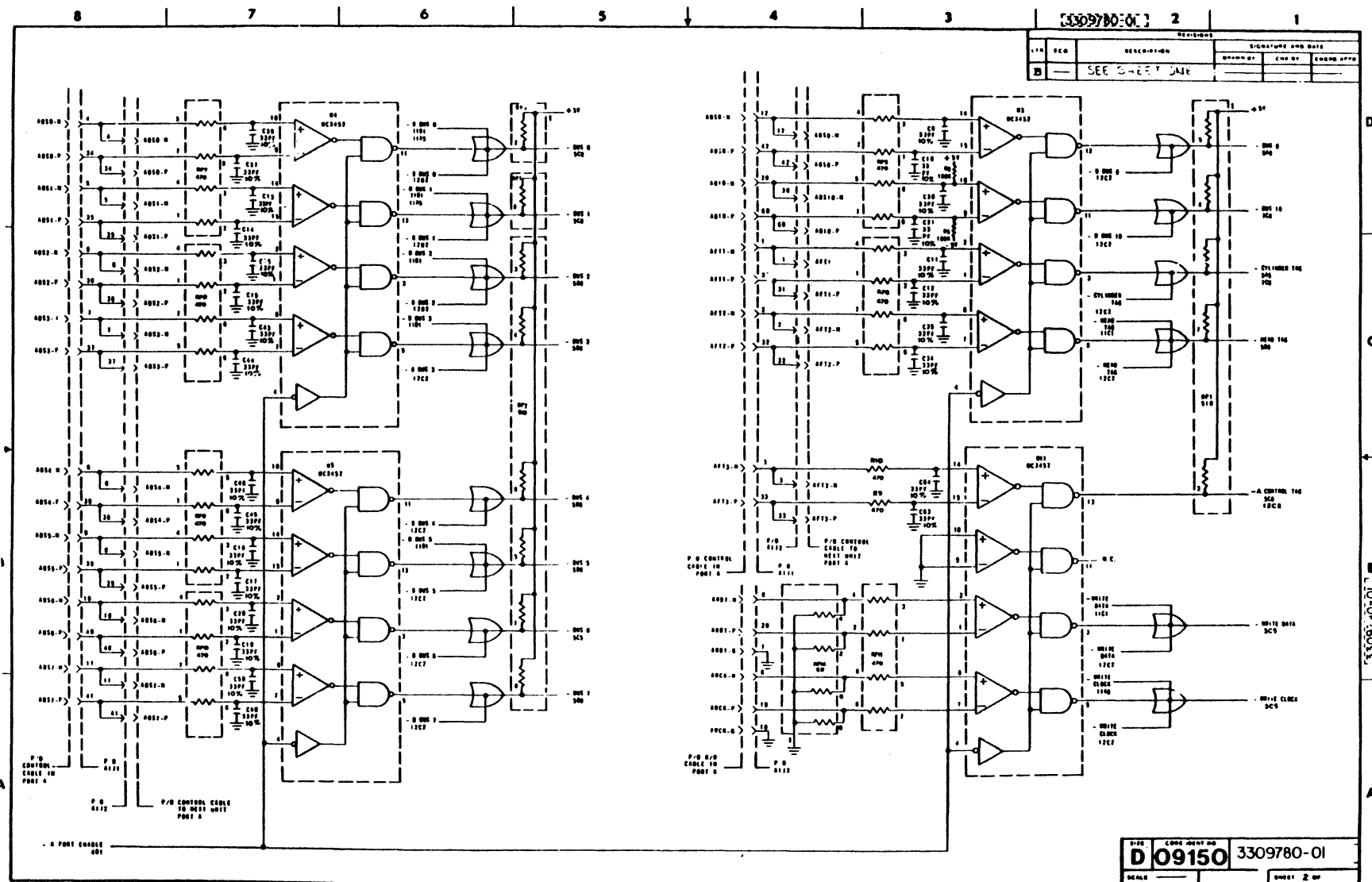
1. Carefully position HDA on chassis pan. Be sure to properly align spindle pulley and spring. A hex driver can be inserted into hole in spring cylinder to hold depressed spring when aligning parts (see Figure 5-14).
2. Tighten three nuts that fasten HDA to chassis pan.
3. Tighten three nuts that fasten drive motor to chassis pan.
4. Reinstall PCBA frame assembly.
5. Reinstall drive belt and drive belt cover.
6. Reinstall top cover.

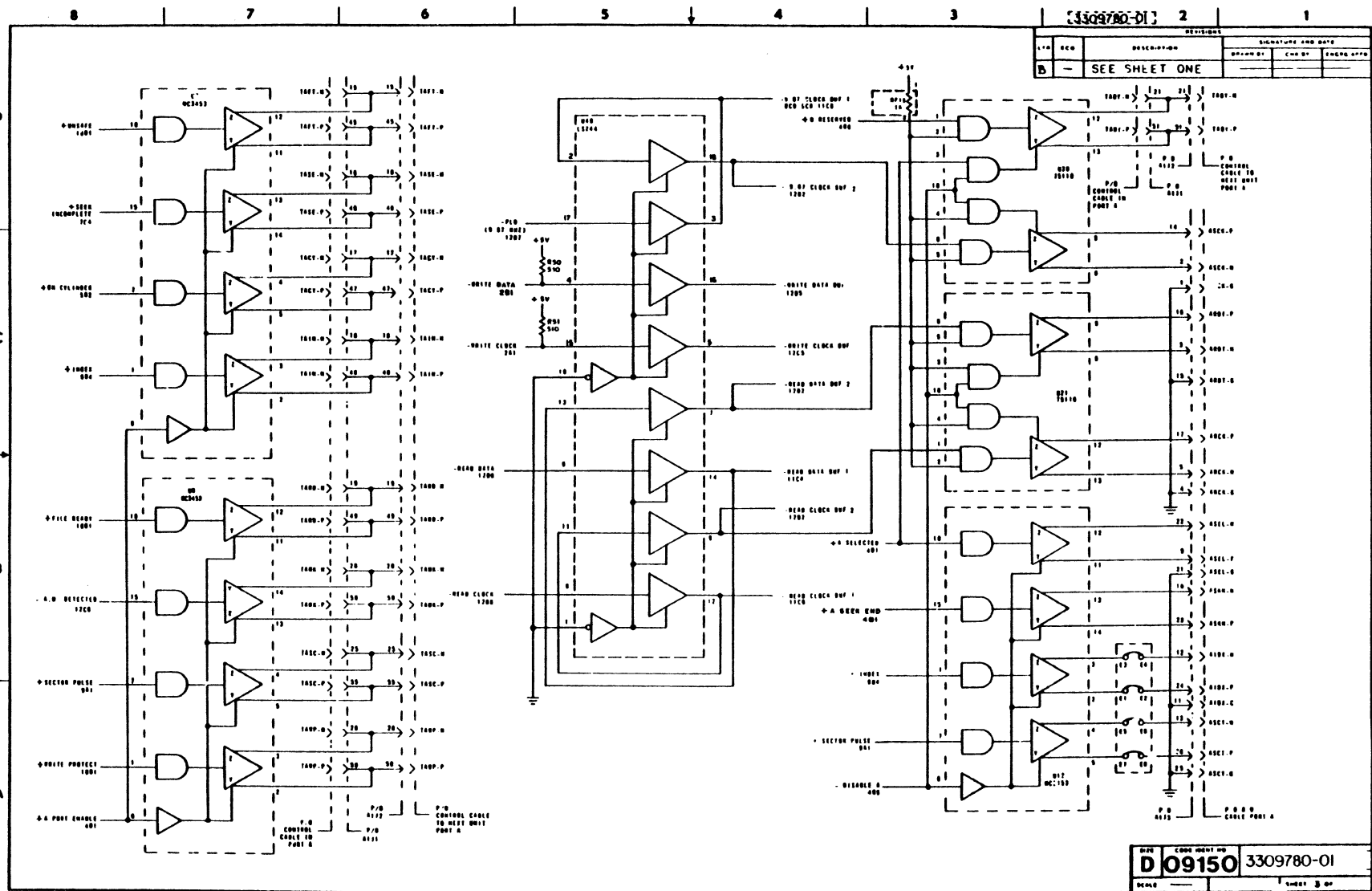
APPENDIX A **REFERENCE DRAWINGS**

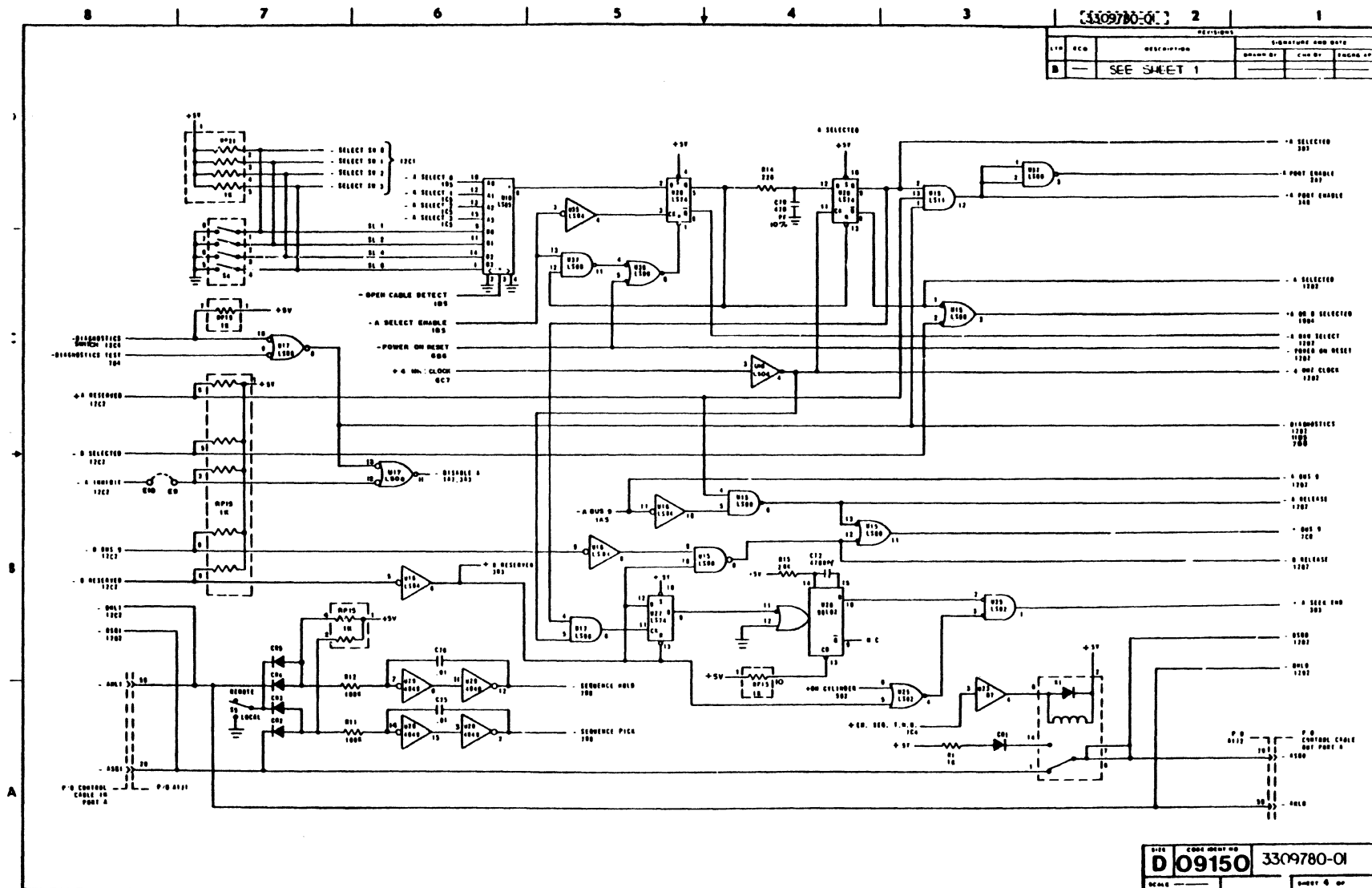
This appendix contains schematic diagrams and assembly drawings for the Capricorn disk drive.

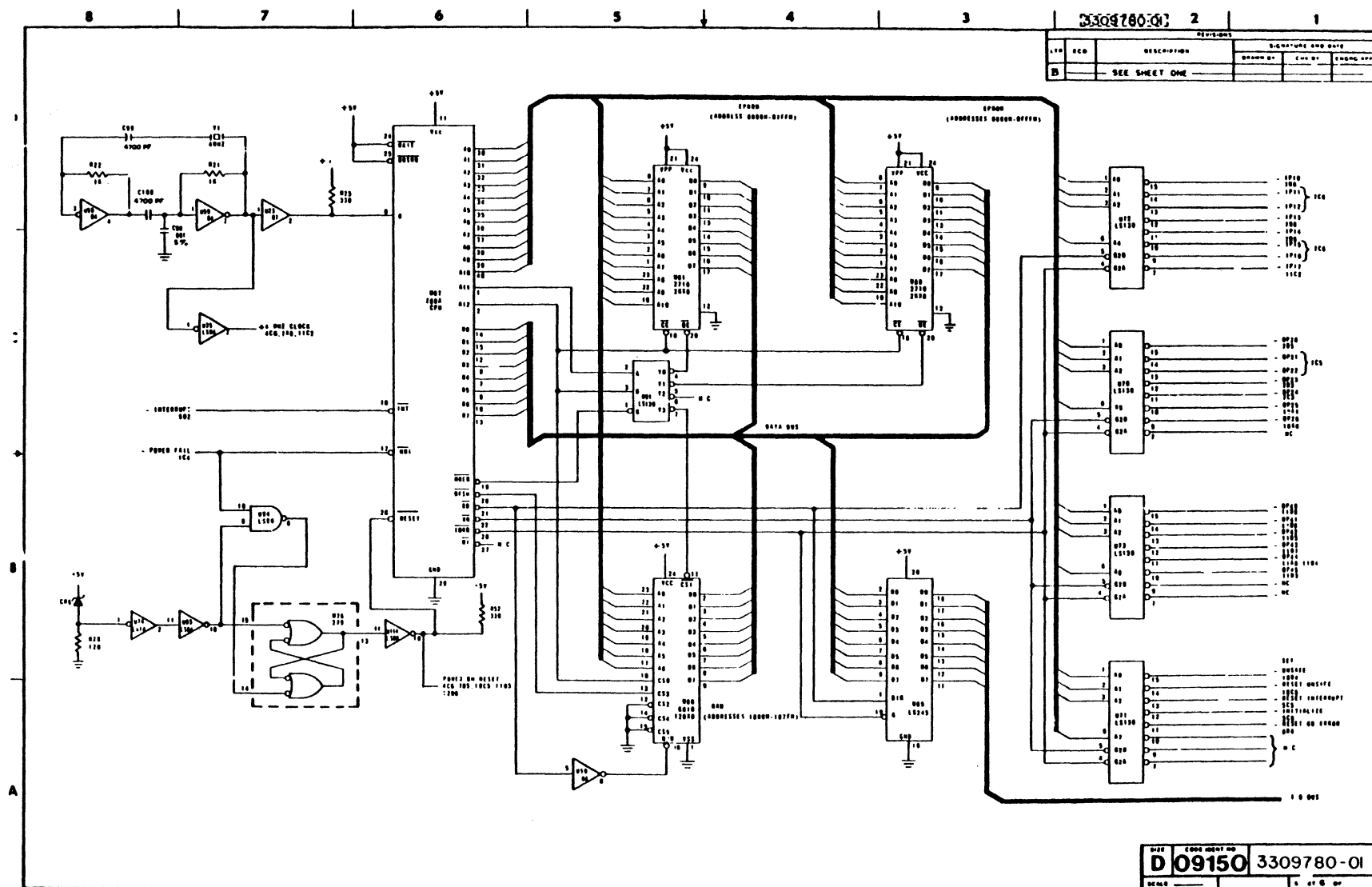
PCBA	Schematic	Rev.	Assy Dwg.	Rev.
I/O and uP Control (A1)	3309780-01	B	3309783-01	B
Read/Write (A2)	3310210-01	D	3310213-01	D
Servo Driver (A3)	3309770-01	D	3309773-01	D
Diagnostic Control Panel (DIC02) (A4)	3310060-01	A	3310063-01	A
Dual-Port Control (A5)	3316180-01	A	3316183	A
Power Supply Regulator (A6)	3309790-01	A	3309793-01	A ¹
HDA Interface (A7)	3309800-01	A	3309803-01	A
Control Cable Termination (TERRC)	3316310	A	3316313	A
Power Distribution	3314455-01	A		
Control Cable, Ribbon Cable Interface			3308179-x x	E
Read/Write Ribbon Cable			3308186-x x	E

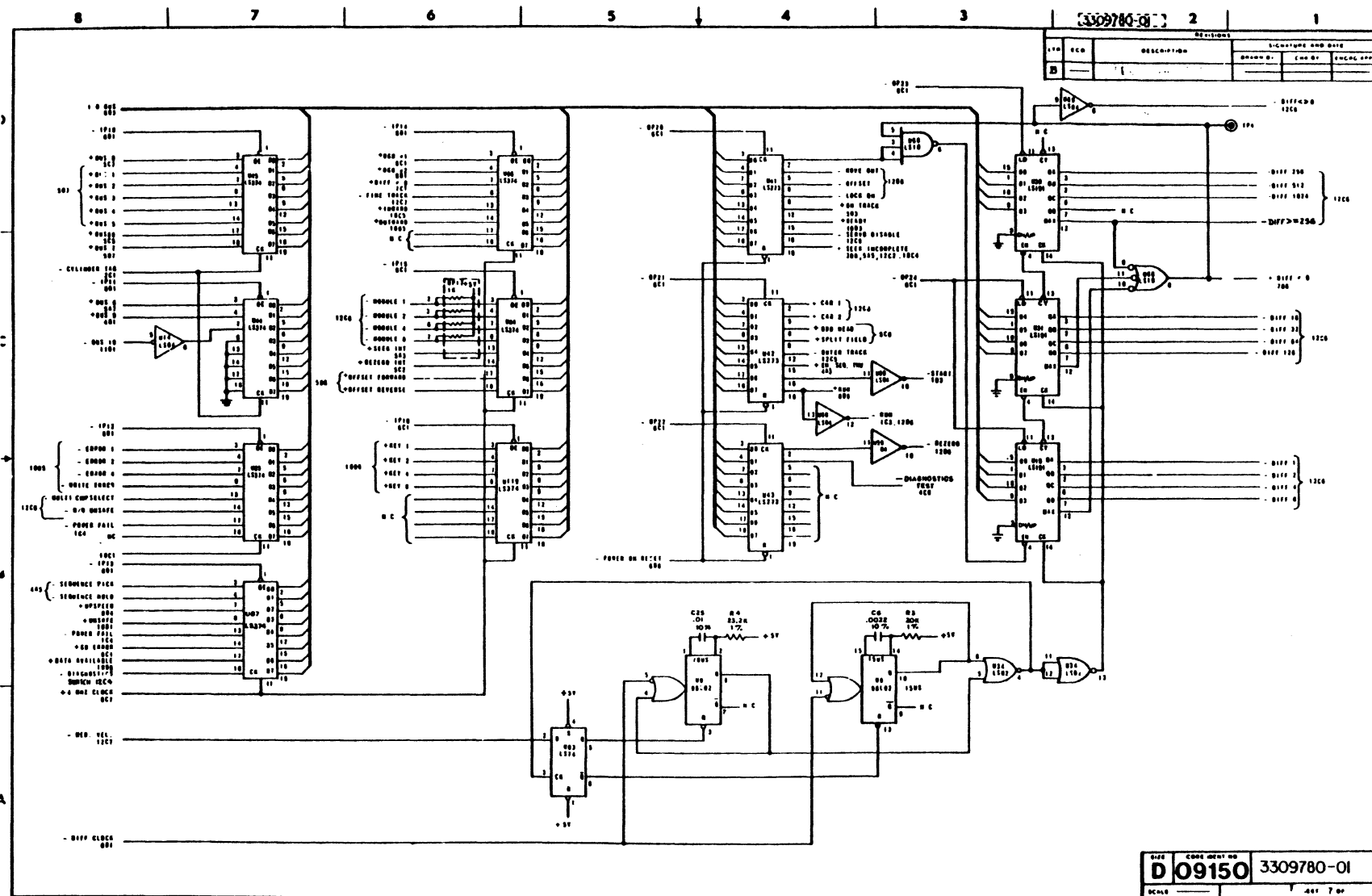


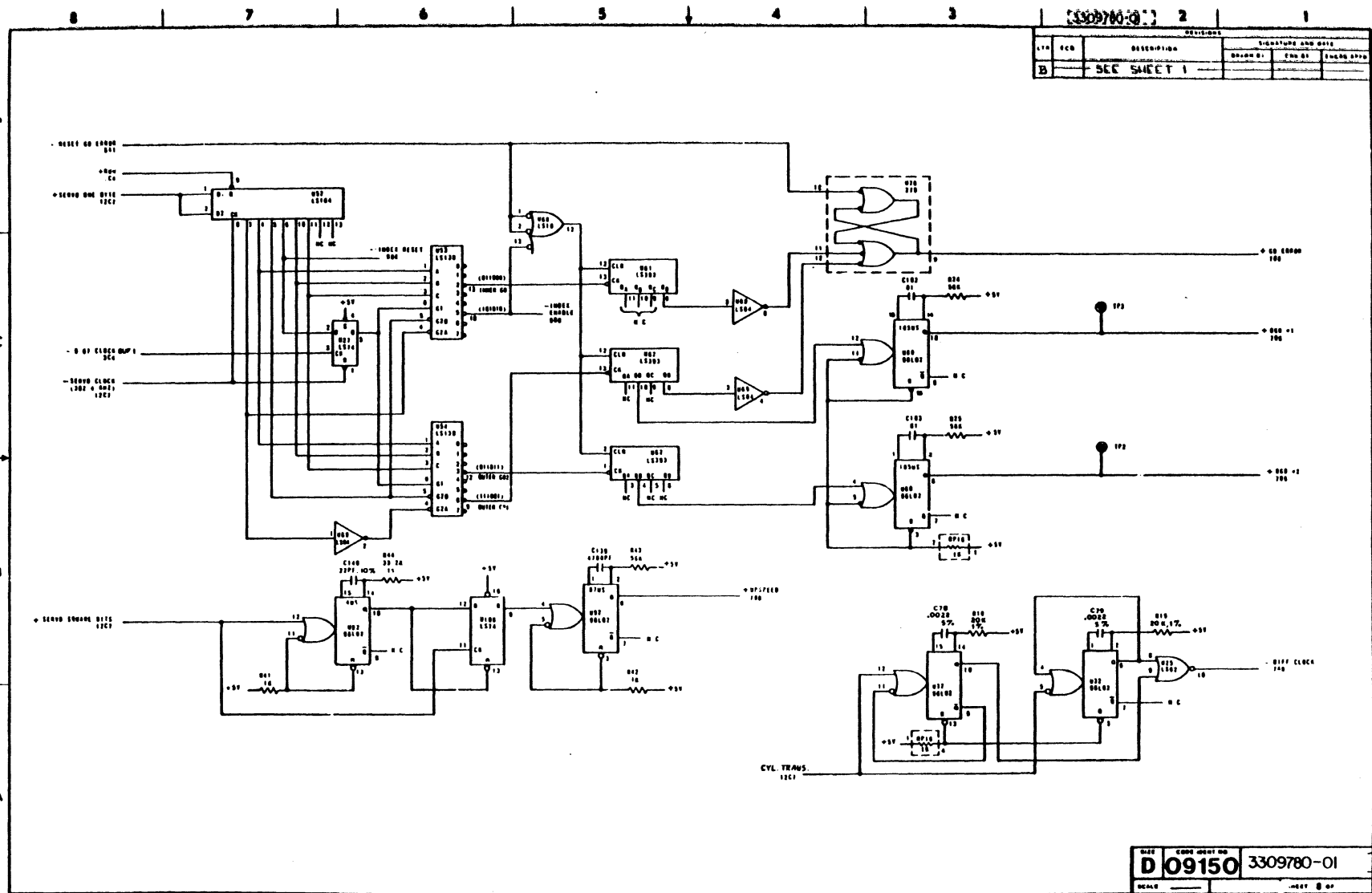


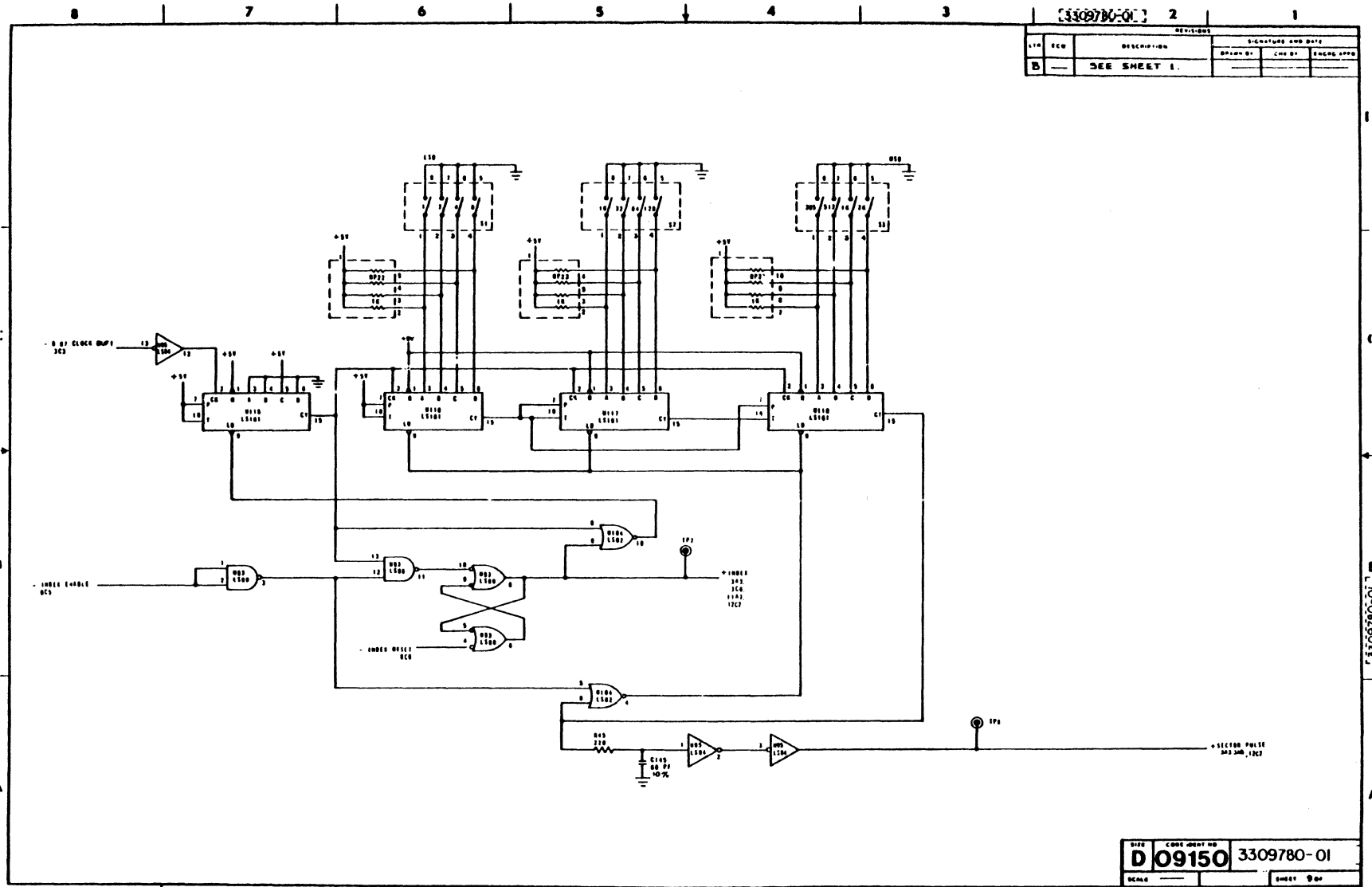


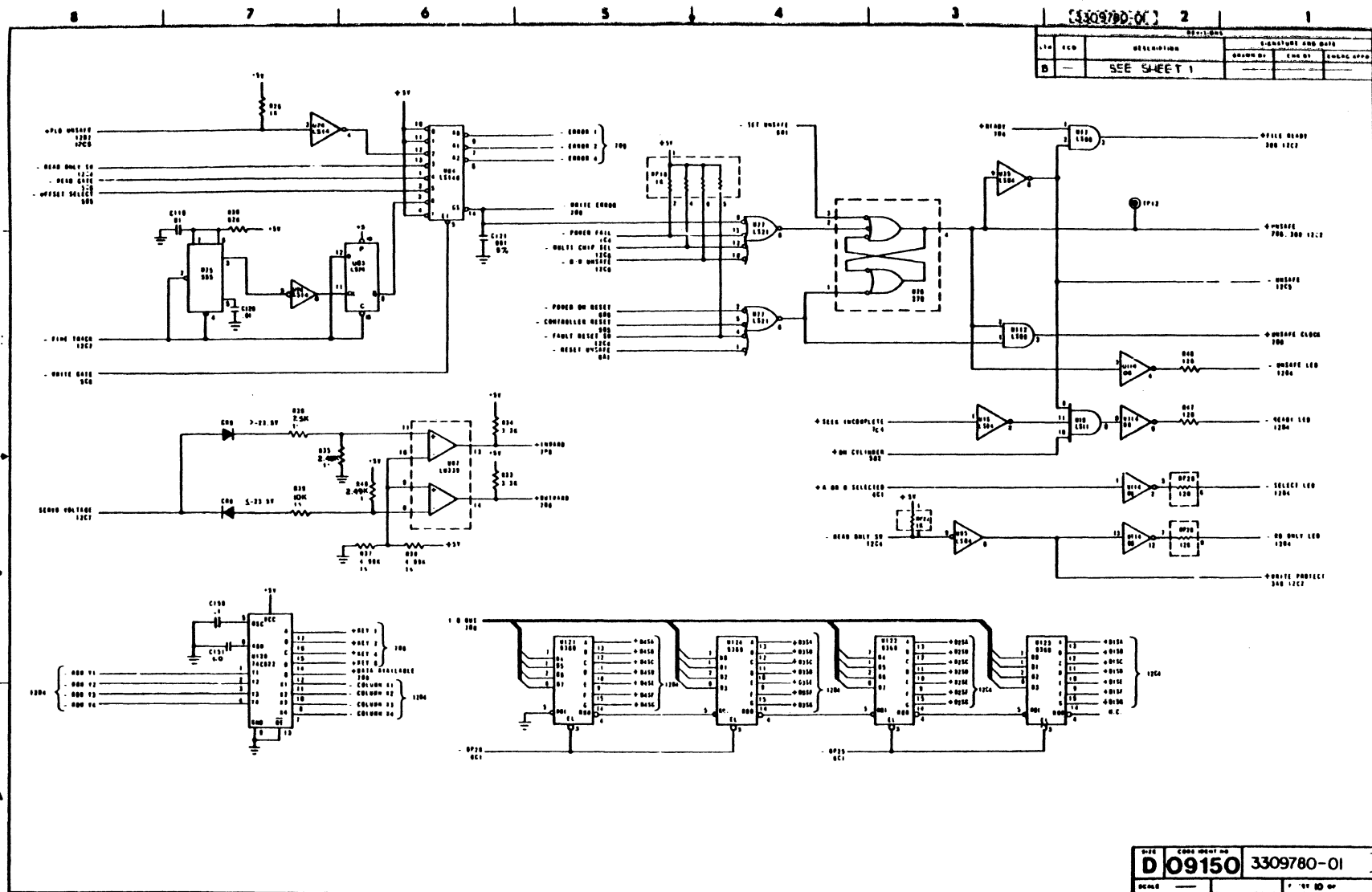


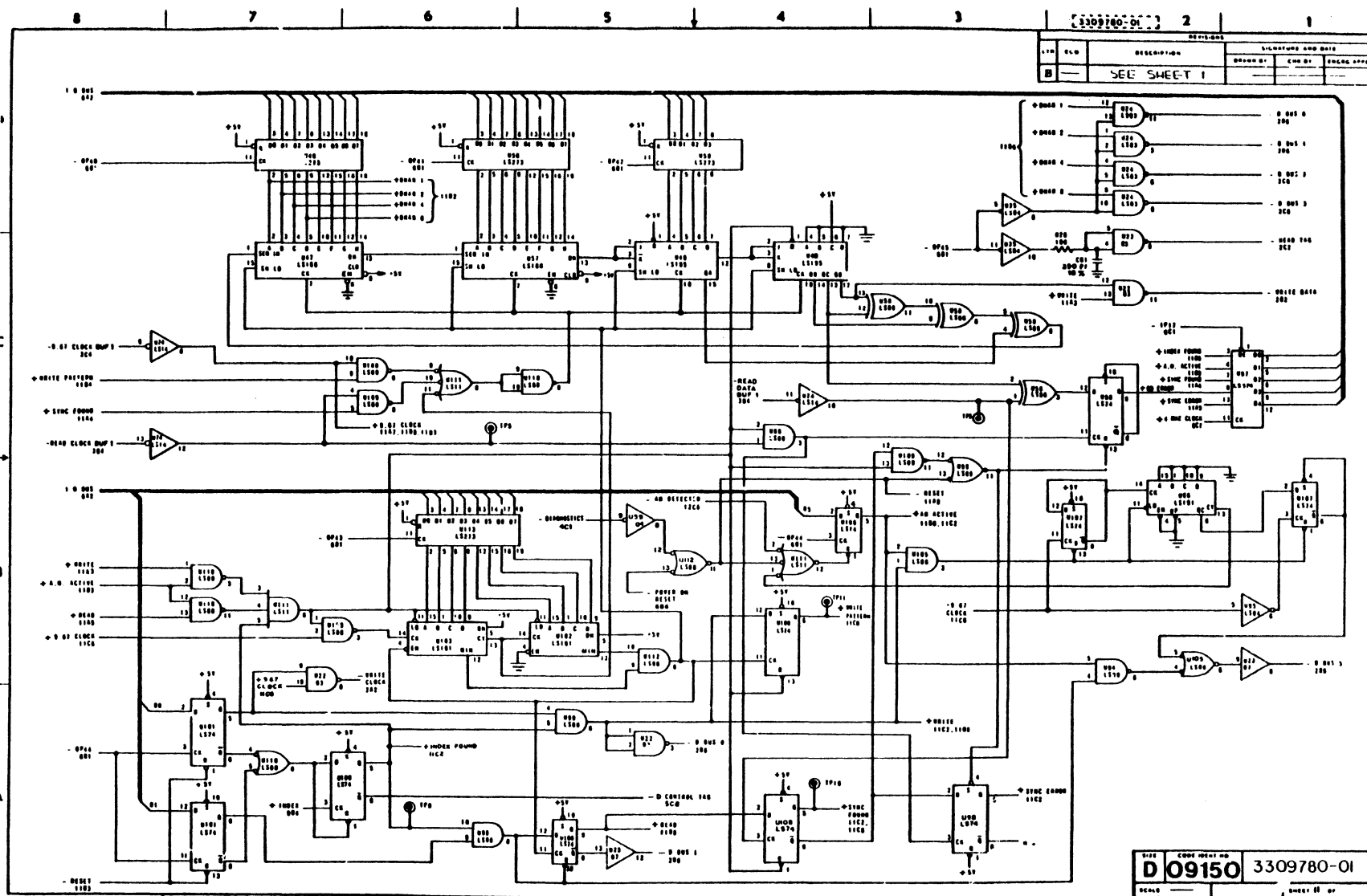




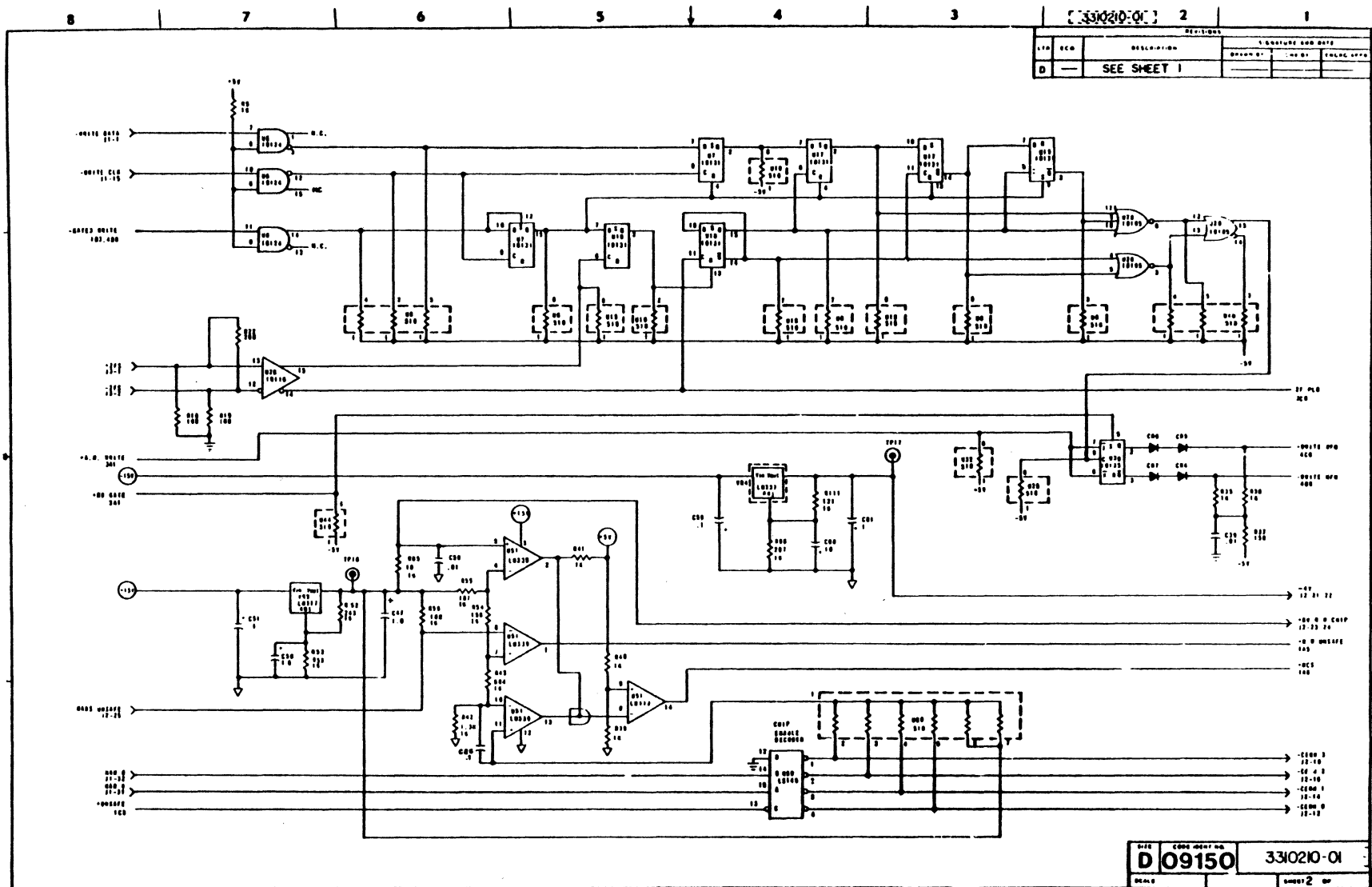


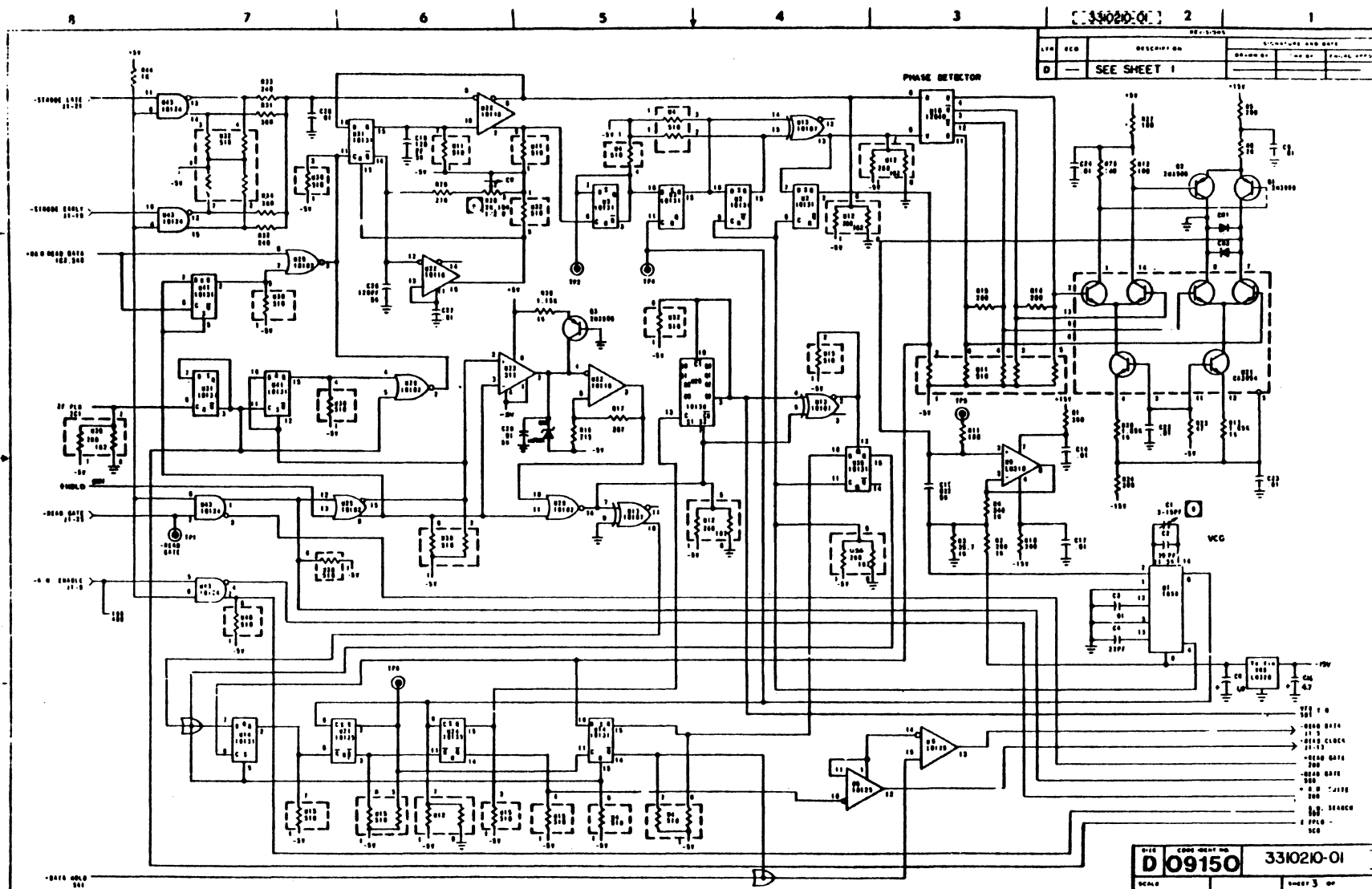


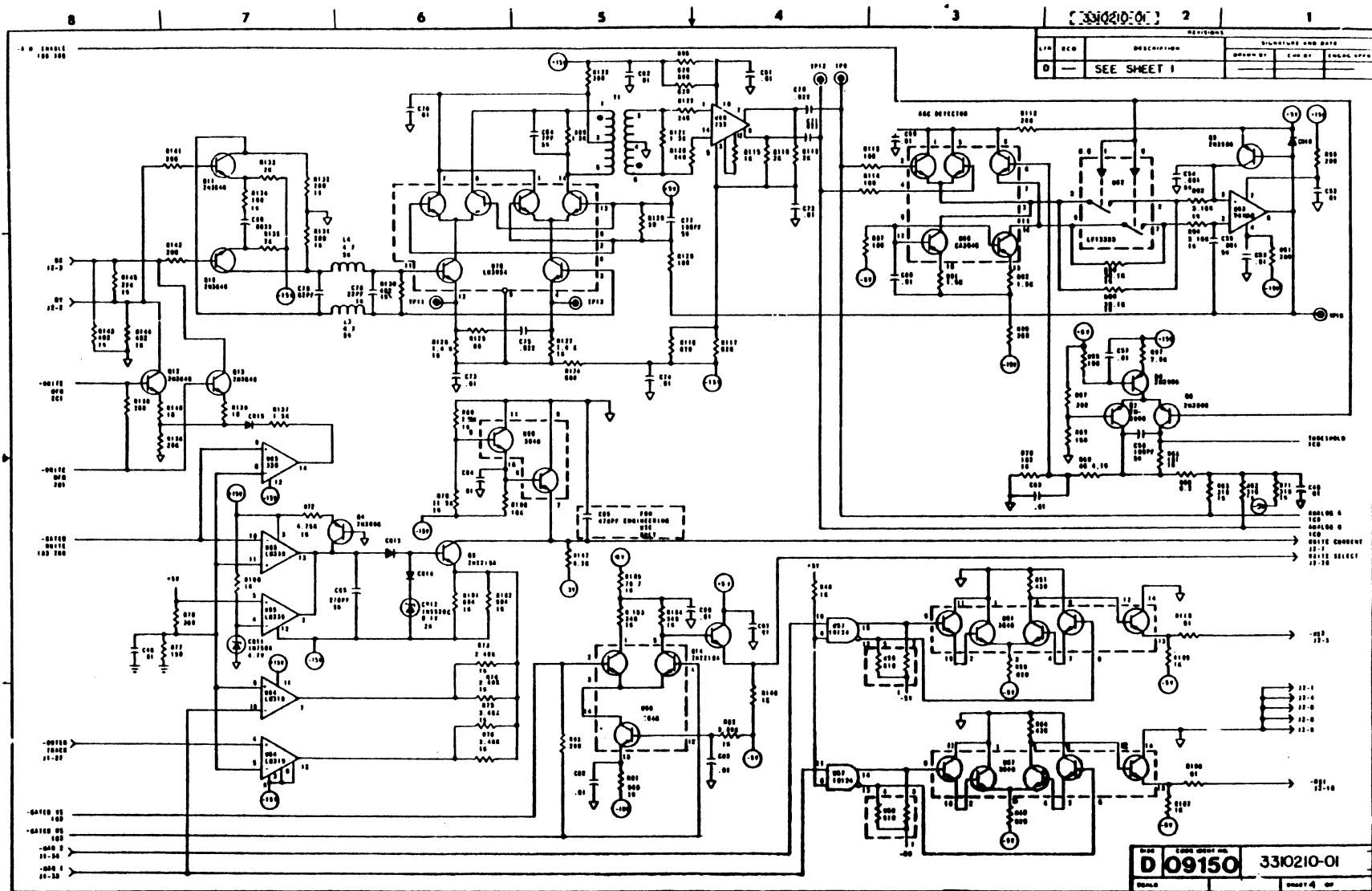


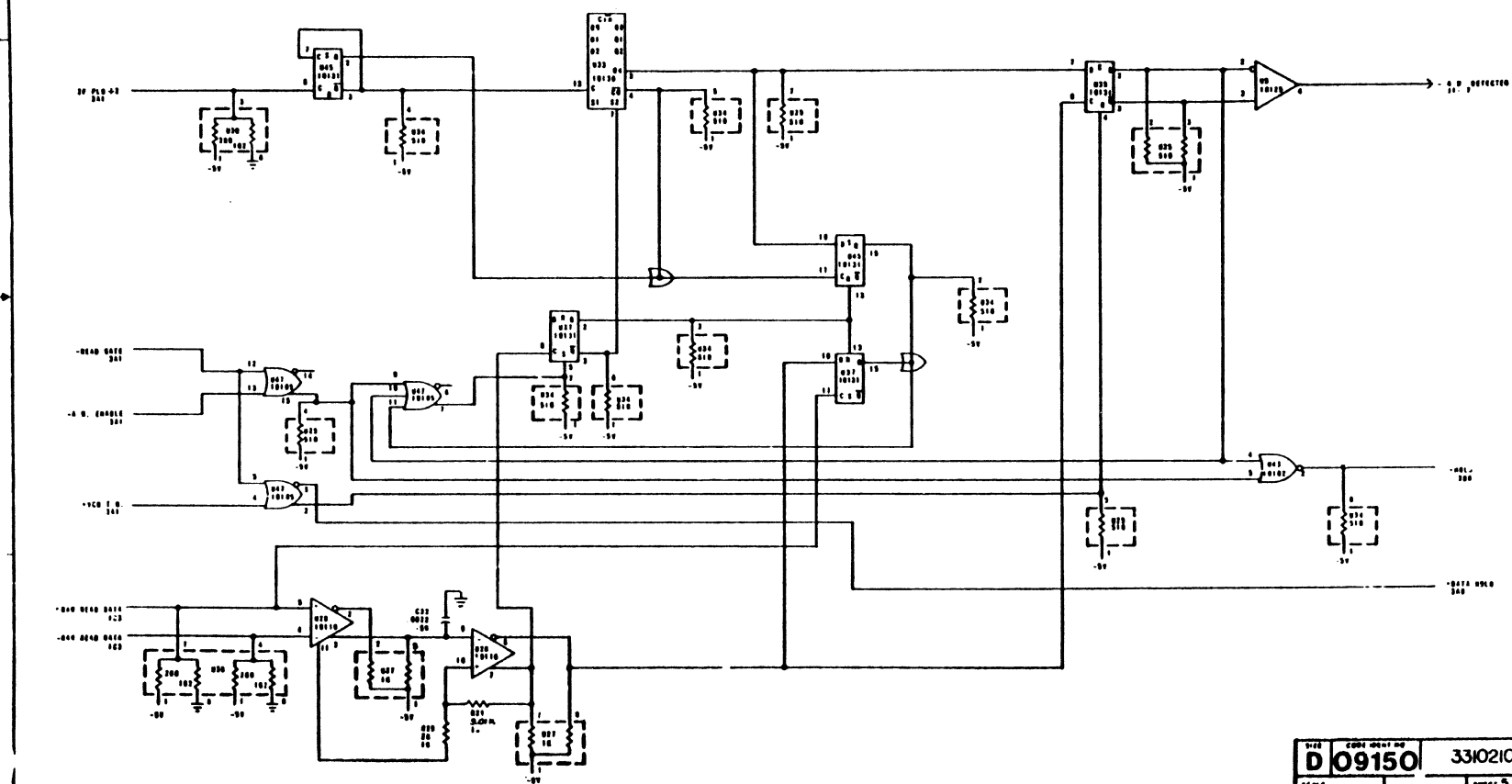


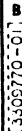
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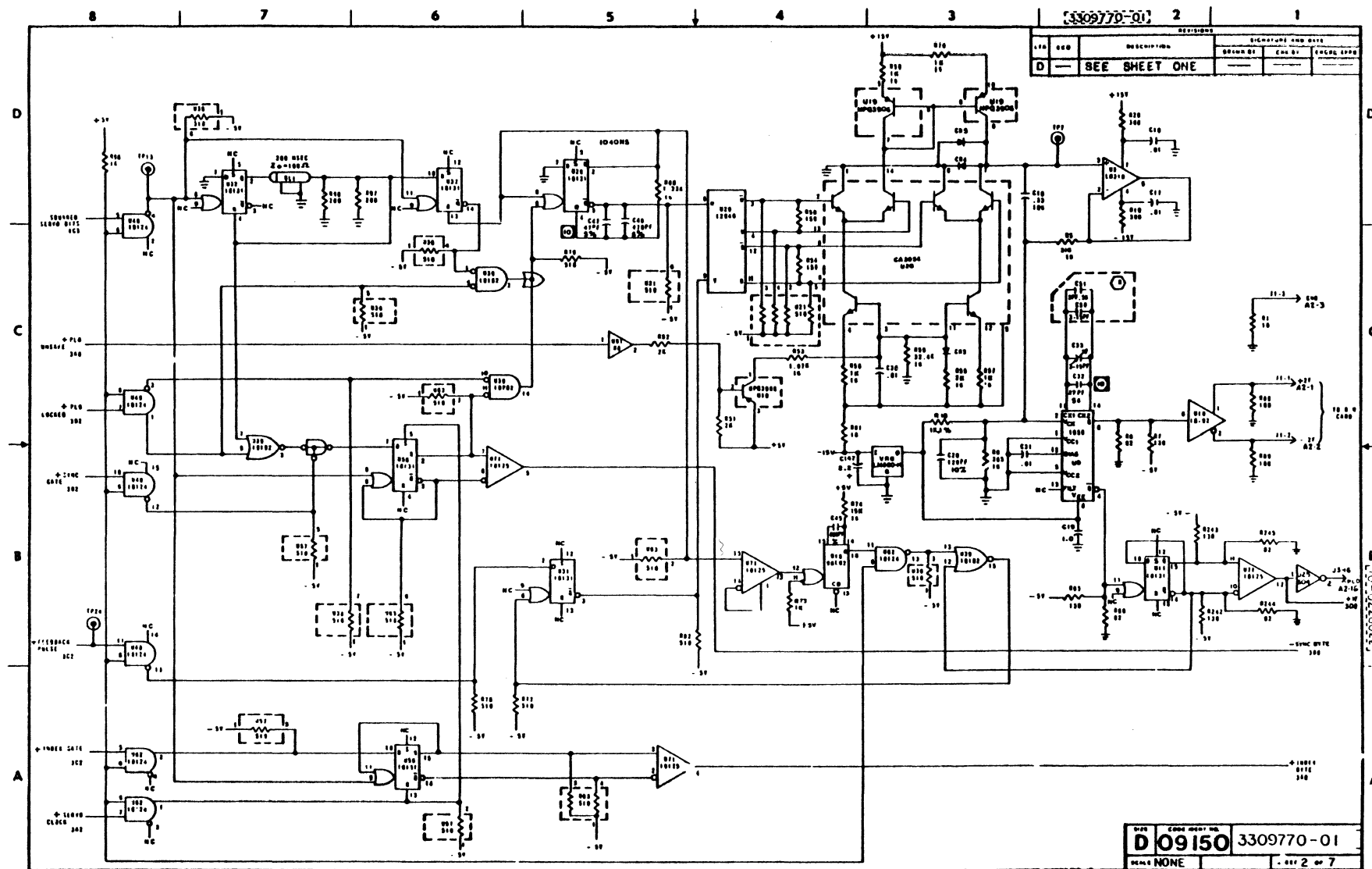


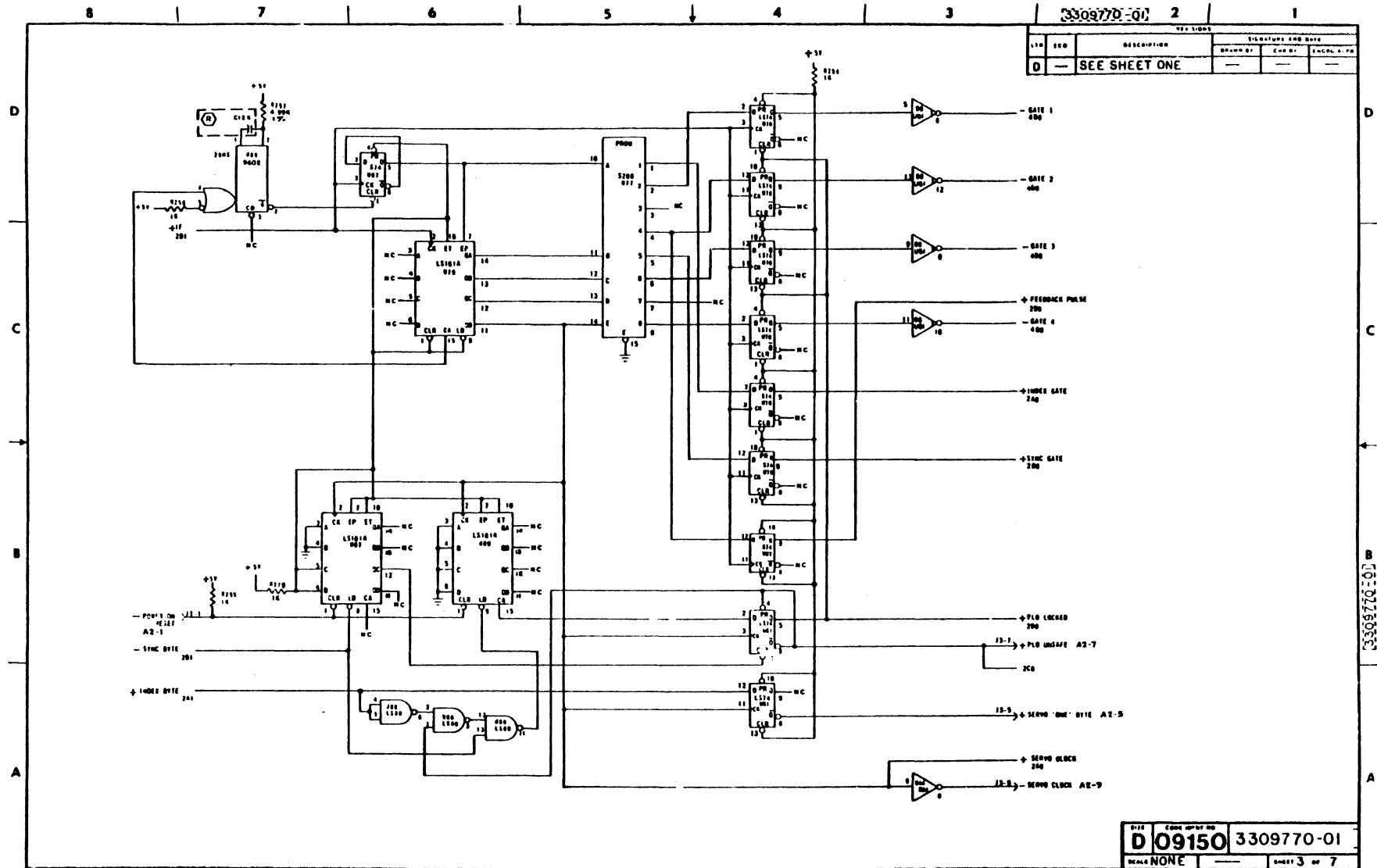


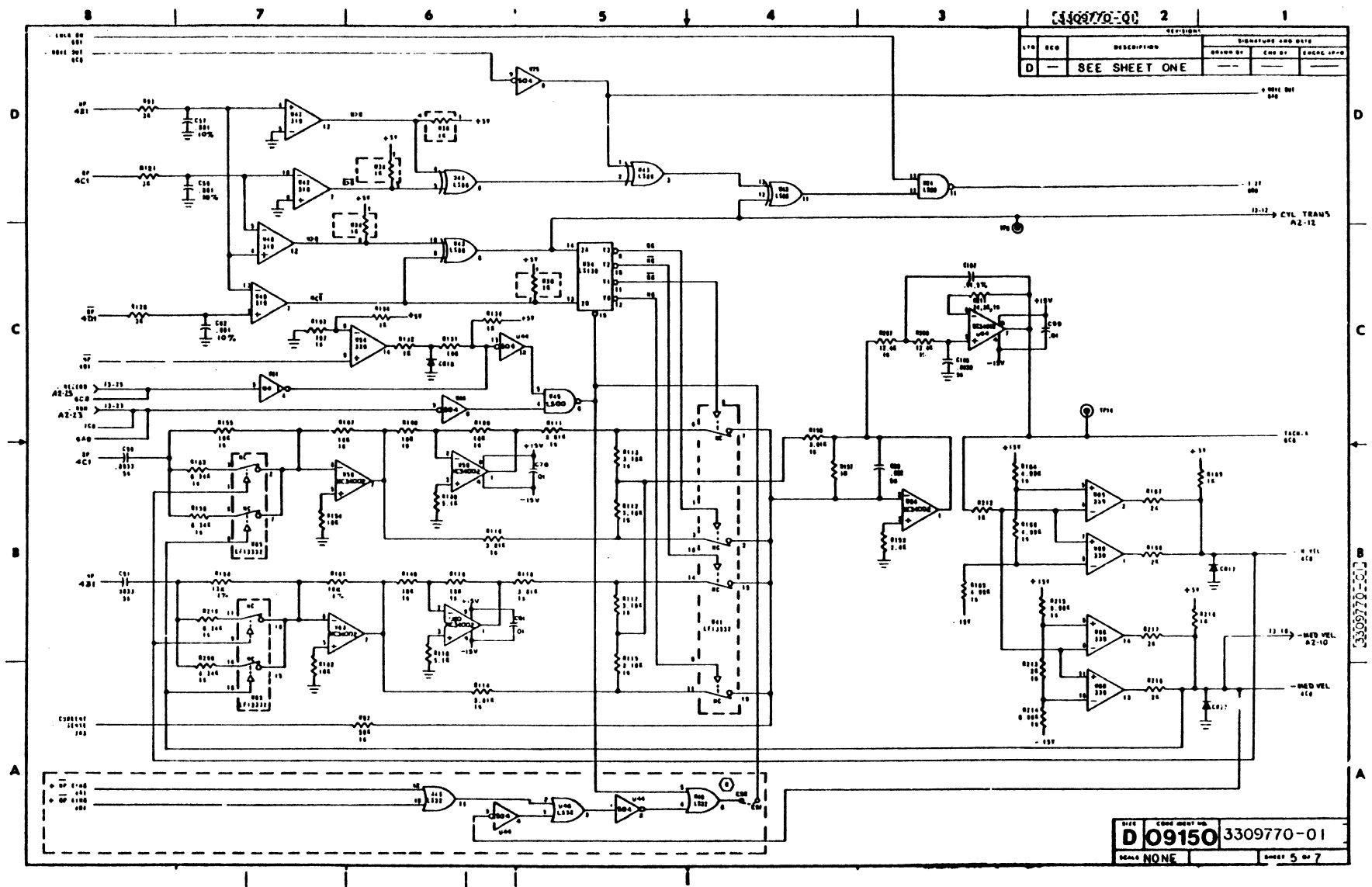


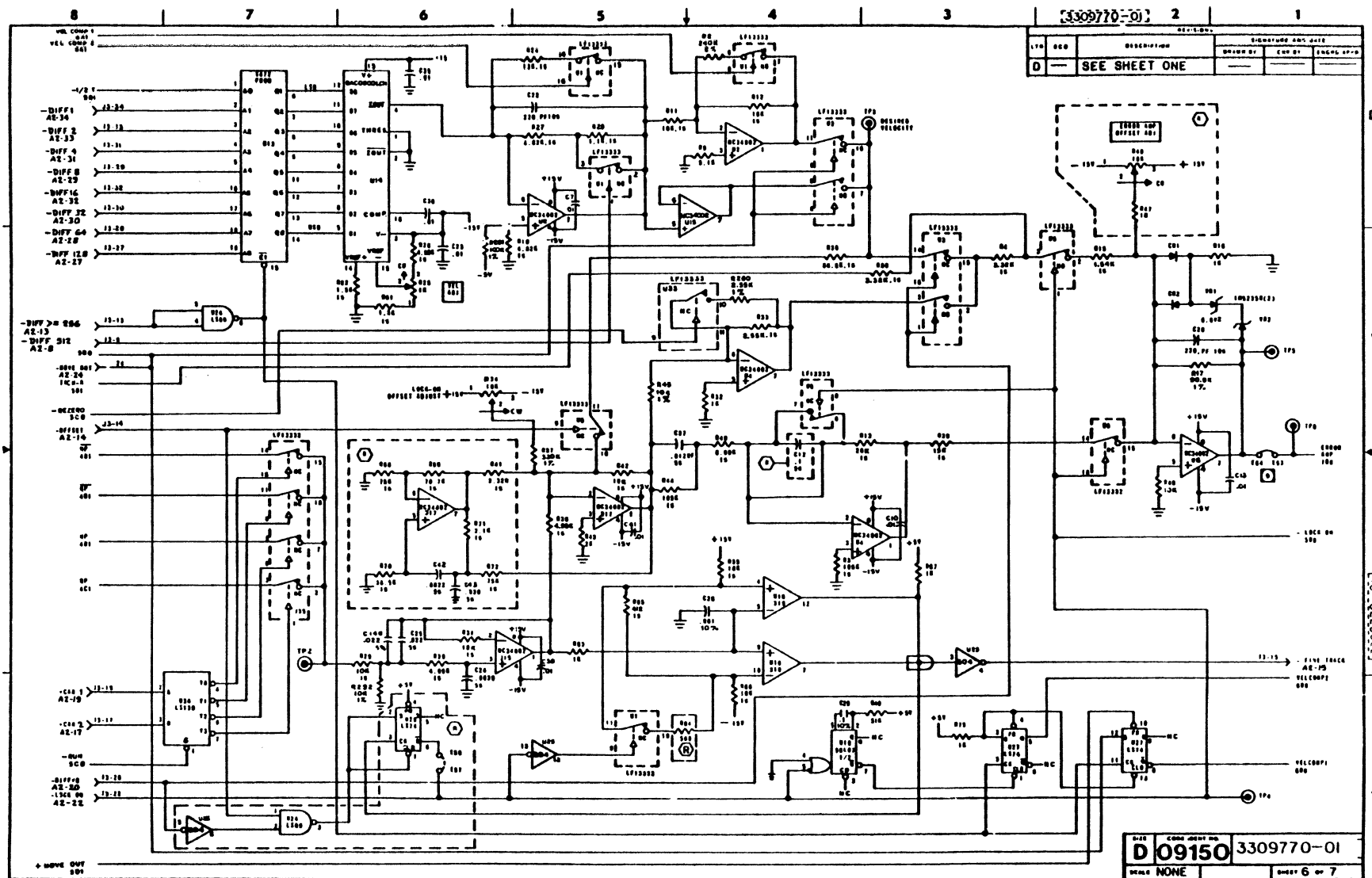


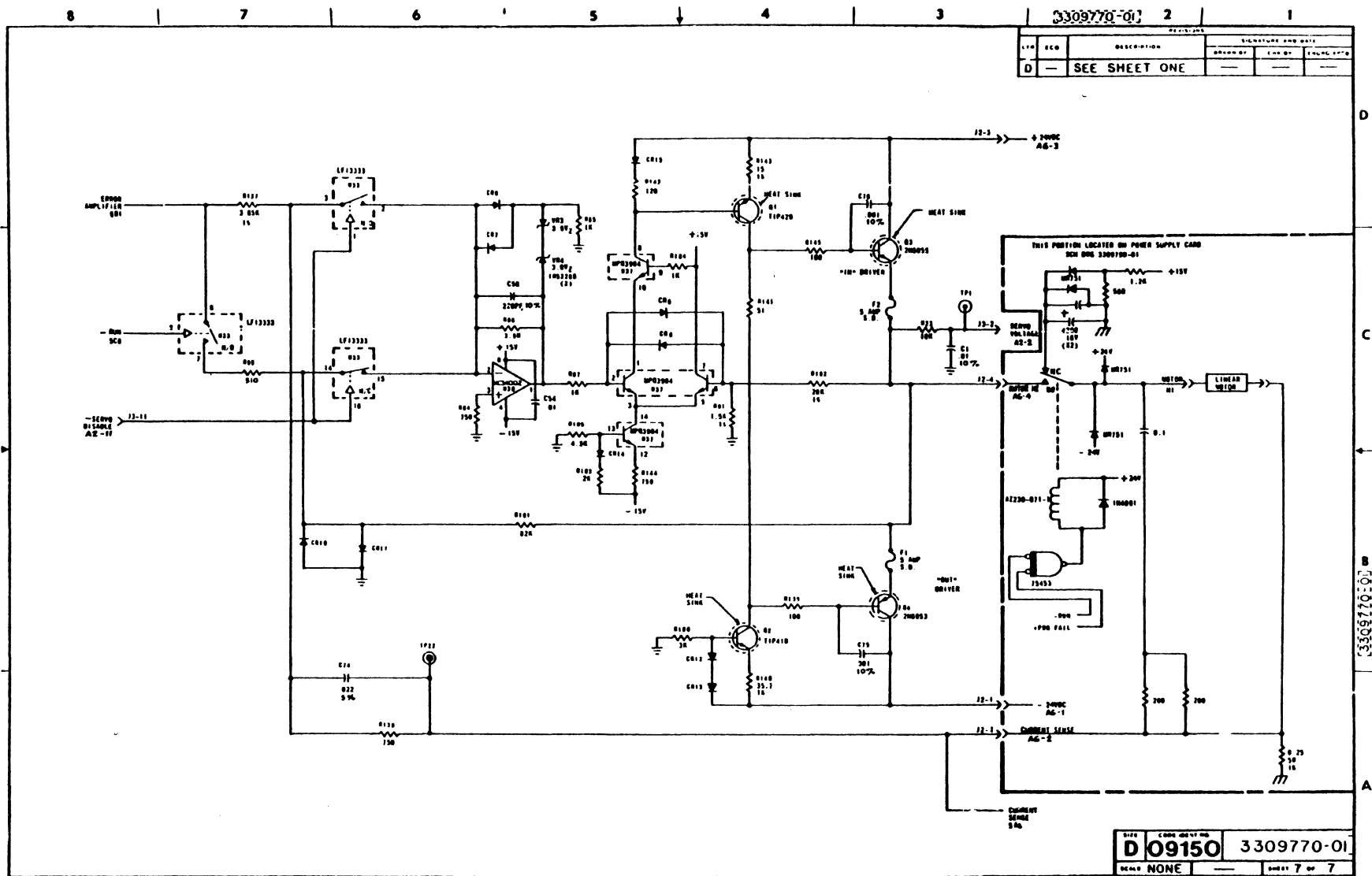












APPENDIX B
LOGIC TERM REFERENCE AIDS

This appendix, consisting of various schematic data, is intended as a reference for the user in locating each signal source and in tracking each signal to all destinations within the drive. Mnemonic terms are defined, along with functional descriptions. Appendix B consists of the following items:

	<u>Page No.</u>
Logic Term Descriptions	B-3
Logic Terms	B-45
Connector-Pin/Component-Pin Terms	B-81
Logic Term Sources	B-115

LOGIC TERM DESCRIPTIONS

This section consists of an alpha-numerical list of the Capricorn disk drive logic terms, term names, and term functions. This reference-only section is intended for use in understanding the logic schematics of Appendix A.

LOGIC TERMS		
Term	Name	Function
- A BUS 9	- A BUS 9	Enabled ABS9 input signal from control unit.
- A CONTROL TAG	- A CONTROL TAG	Enabled AFT3 input signal for Port A.
- A INHIBIT	- A INHIBITED	Port A inhibit signal generated by priority logic.
+ A OR B SELECTED	A OR B SELECTED	Signal generated by Select logic to drive A4DS5 (SELECTED indicator).
+ A PORT ENABLE	+ A PORT ENABLE	Signal generated by Port A Select logic to enable Port A receivers and transmitters.
- A PORT ENABLE	- A PORT ENABLE	Signal generated by Port A Select logic to enable Port A receivers and transmitters.
- A PRIORITY	- A PRIORITY	Clears Port A 500 ms release timer flip-flop.
- A RAW SELECT	- A RAW SELECT	Asynchronous Port A selected signal used to clock Port A priority logic.

LOGIC TERMS

Term	Name	Function
-1/2T	ONE-HALF TIME PERIOD	Factor signal obtained from cylinder generator circuit for use by desired velocity circuit.
+1F	+1 FREQUENCY	PLO clock used to sync servo timing logic.
2 FPLO -(2 FPLO +2)	2 FREQUENCY PHASE LOCK OSCILLATOR	2FPLO (19.34 MHz) +2 = 9.6 MHz clock.
+2F (+2 FS)	+2 FREQUENCY	VCO output clock (19.34 MHz) used as strobe in the write encoder circuit.
-2F (-2 FS)	-2 FREQUENCY	VCO output clock (19.34 MHz) used as strobe in the write encoder circuit.
2F PLO	2 FREQUENCY	Inverted VCO output (See -2F)
-4 MHZ CLOCK	-4 MEGAHERTZ CLOCK	Microprocessor and control timing clock.
+4 MHZ CLOCK	+4 MEGAHERTZ CLOCK	Microprocessor and control timing clock.
+4V	+4V READ/WRITE CHIP	Supply voltage to read/write IC chip.
+6V R/W CHIP	+6 VOLTS READ/WRITE CHIP	Supply voltage (VCC) to read/write IC chip.
+9.67 CLOCK	+9.67 CLOCK	Compliment of signal -9.67 CLOCK BUF 1; used to sync internal circuits.
-9.67 CLOCK BUF 1	-9.67 CLOCK BUFFER 1	PLO output used to sync drive circuits; also used as source for fan out signal -9.67 CLOCK BUF 2.
-9.67 CLOCK BUF 2 (-9.67 CLK)	-9.67 CLOCK BUFFER 2	PLO output used as source for fan out signal ASCK and BSCK.
-A BUS 9	-A BUS 9	Enabled ABS9 input signal from control unit.
-A CONTROL TAG	-A CONTROL TAG	Enabled AFT3 input signal for Port A.
-A INHIBIT	-A INHIBITED	Port A inhibit signal generated by priority logic.

LOGIC TERMS (Cont.)

Term	Name	Function
-A OR B SELECTED	A or B SELECTED	Signal generated by Select logic to drive A4DS5 (SELECTED indicator).
+A PORT ENABLE	+A PORT ENABLE	Signal generated by Port A Select logic to enable some Port A receivers and transmitters.
-A PORT ENABLE	-A PORT ENABLE	Signal generated by Port A Select logic to enable some Port A receivers and transmitters.
-A PRIORITY	-A PRIORITY	Clears Port A 500 ms release timer flip-flop. Inhibits timer when priority selected by Port A.
-A RAW SELECT	-A RAW SELECT	Asynchronous Port A selected signal used to clock Port A priority logic.
-A RELEASE	-A RELEASE	Product of signals A Reserved and A Bus 9, used to gate A control tag.
+A RESERVED	+A RESERVED	Active when Port A is selected and/or reserved.
-A SELECT 0	-A SELECT 0	One of four binary coded unit selection lines. See paragraph 4.3.3.
-A SELECT 1	-A SELECT 1	One of four binary coded unit selection lines. See paragraph 4.3.3.
-A SELECT 2	-A SELECT 2	One of four binary coded unit selection lines. See paragraph 4.3.3.
-A SELECT 3	-A SELECT 3	One of four binary coded unit selection lines. See paragraph 4.3.3.
-A SELECT ENABLE	-A SELECT ENABLE	When active, this signal permits binary decoding of Port A Device Select lines. See paragraph 4.3.2.

LOGIC TERMS (Cont.)

Term	Name	Function
-A SELECTED	-A SELECTED	Used to enable one transmitter and is source signal for terms ASEL-N and ASEL-P (selected status to controller).
+A SELECTED	+A SELECTED	Used to enable receivers and transmitters and as input to Reserve logic.
ABS0-N	A BUS 0-NEG	Port A Bus Out 0 —Signal function determined by configuration of function-tag control lines (see paragraph 4.3).
ABS0-P	A BUS 0-POS	Port A Bus Out 0 —Signal function determined by configuration of function-tag control lines (see paragraph 4.3).
ABS1-N	A BUS 1-NEG	Port A Bus Out 1 —Signal function determined by configuration of function-tag control lines (see paragraph 4.3).
ABS1-P	A BUS 1-POS	Port A Bus Out 1 —Signal function determined by configuration of function-tag control lines (see paragraph 4.3).
ABS10-N	A BUS 10-NEG	Port A Bus Out 10 (DM9160). See paragraph 4.3.6.
ABS10-P	A BUS 10-POS	Port A Bus Out 10 (DM9160). See paragraph 4.3.6.
ABS2-N	A BUS 2-NEG	Port A Bus Out 2 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS2-P	A BUS 2-POS	Port A Bus Out 2 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).

LOGIC TERMS (Cont.)

Term	Name	Function
ABS3-N	A BUS 3-NEG	Port A Bus Out 3 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS3-P	A BUS 3-POS	Port A Bus Out 3 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS4-N	A BUS 4-NEG	Port A Bus Out 4 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS4-P	A BUS 4-POS	Port A Bus Out 4 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS5-N	A BUS 5-NEG	Port A Bus Out 5 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS5-P	A BUS 5-POS	Port A Bus Out 5 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS6-N	A BUS 6-NEG	Port A Bus Out 6 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS6-P	A BUS 6-POS	Port A Bus Out 6 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS7-N	A BUS 7-NEG	Port A Bus Out 7 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).

LOGIC TERMS (Cont.)

Term	Name	Function
ABS7-P	A BUS 7-POS	Port A Bus Out 7 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS8-N	A BUS 8-NEG	Port A Bus Out 8 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS8-P	A BUS 8-POS	Port A Bus Out 8 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS9-N	A BUS 9-NEG	Port A Bus Out 9 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
ABS9-P	A BUS 9-POS	Port A Bus Out 9 —Signal function is determined by configuration of function-tag control lines (see paragraph 4.3).
-ADDRESS MARK ENABLE (-AM ENABLE)	-ADDRESS MARK ENABLE	When active during write, this signal prevents write data from going to write drivers; during Write AM, prevents R/W Unsafe; and during AM Search, changes AGC. When active during Read this signal becomes AM Search.
AFT1-N	A FUNCTION TAG 1-NEG	Port A Cylinder Select (Tag 1). See paragraph 4.3.4.
AFT1-P	A FUNCTION TAG 1-POS	Port A Cylinder Select (Tag 1). See paragraph 4.3.4.
AFT2-N	A FUNCTION TAG 2-NEG	Port A Head Select (Tag 2). See paragraph 4.3.5.
AFT2-P	A FUNCTION TAG 2-POS	Port A Head Select (Tag 2). See paragraph 4.3.5.
AFT3-N	A FUNCTION TAG 3-NEG	Port A Control Select (Tag 3). See paragraph 4.3.6.

LOGIC TERMS (Cont.)

Term	Name	Function
AFT3-P	A FUNCTION TAG 3-POS	Port A Control Select (Tag 3). See paragraph 4.3.6.
+2FS (+2F)	+TWICE FREQUENCY PLO CLOCK	VCO output clock (19.4) used as strobe in the Write Encoder circuit.
-2FS (-2F)	-TWICE FREQUENCY PLO CLOCK	VCO output clock (19.4) used as strobe in the Write Encoder circuit.
AGC	AUTOMATIC GAIN CONTROL	Compensates for difference in signal amplitude from outer to inner cylinders to provide overall constant gain.
-AHL I	-A HOLD IN	Port A Power Sequence Hold. See paragraph 4.13.15.
-AHL O	-A HOLD OUT	Port A Power Sequence Hold. See paragraph 4.13.15.
AIDX-N	A INDEX-NEG	Port A Reserved for Index pulse obtained from servo tracks. See paragraph 4.4.7.
AIDX-P	A INDEX-POS	Port A Reserved for Index pulse obtained from servo tracks. See paragraph 4.4.7.
+AM ACTIVE	+ADDRESS MARK ACTIVE	Prevents write data from going to write driver circuits.
-AM DETECTED	-ADDRESS MARK DETECTED	Active when AM detect circuit counts absence of 16 consecu- tive MFM data bits.
-AM ENABLE (-ADDRESS MARK ENABLE)	(SEE ADDRESS MARK ENABLE)	
-AM SEARCH	-ADDRESS MARK SEARCH	When active, this signal enables AM detection circuit. See paragraph 4.13.14.
+AM WRITE	+ADDRESS MARK WRITE	When active, this signal prevents the transfer of write data to the write drivers.
ANALOG A	ANALOG A	Automatic gain control dif- ference signals to read detector.

LOGIC TERMS (Cont.)

Term	Name	Function
ANALOG B	ANALOG B	Automatic gain control difference signals to read detector.
ARCK-N	A READ CLOCK-NEG	Port A Read Clock. See paragraph 4.4.1.
ARCK-P	A READ CLOCK-POS	Port A Read Clock. See paragraph 4.4.1.
ARDT-N	A READ DATA-NEG	Port A Read Data. See paragraph 4.4.2.
ARDT-P	A READ DATA-POS	Port A Read Data. See paragraph 4.4.2.
ARDV-N	A RECEIVE DEVICE-NEG	Port A Device Enable (Open Cable Detect). See paragraph 4.3.1.
ARDV-P	A RECEIVE DEVICE-POS	Port A Device Enable (Open Cable Detect). See paragraph 4.3.1.
ARSO-N	A RECEIVE SELECT 0-NEG	Port A Unit Select (2 ⁰). See paragraph 4.3.3.
ARSO-P	A RECEIVE SELECT 0-POS	Port A Unit Select (2 ⁰). See paragraph 4.3.3.
ARS1-N	A RECEIVE SELECT 1-NEG	Port A Unit Select (2 ¹). See paragraph 4.3.3.
ARS1-P	A RECEIVE SELECT 1-POS	Port A Unit Select (2 ¹). See paragraph 4.3.3.
ARS2-N	A RECEIVE SELECT 2-NEG	Port A Unit Select (2 ²). See paragraph 4.3.3.
ARS2-P	A RECEIVE SELECT 2-POS	Port A Unit Select (2 ²). See paragraph 4.3.3.
ARS3-N	A RECEIVE SELECT 3-NEG	Port A Unit Select (2 ³). See paragraph 4.3.3.
ARS3-P	A RECEIVE SELECT 3-POS	Port A Unit Select (2 ³). See paragraph 4.3.3.
ARSL-N	A RECEIVE SELECT-NEG	Port A Select Enable (Unit Select Tag). See paragraph 4.3.2.
ARSL-P	A RECEIVE SELECT-POS	Port A Select Enable (Unit Select Tag). See paragraph 4.3.2.

LOGIC TERMS (Cont.)

Term	Name	Function
AFT3-P	A FUNCTION TAG 3-POS	Port A Control Select (Tag 3). See paragraph 4.3.6.
+2FS (+2F)	+TWICE FREQUENCY PLO CLOCK	VCO output clock (19.4) used as strobe in the Write Encoder circuit.
-2FS (-2F)	-TWICE FREQUENCY PLO CLOCK	VCO output clock (19.4) used as strobe in the Write Encoder circuit.
AGC	AUTOMATIC GAIN CONTROL	Compensates for difference in signal amplitude from outer to inner cylinders to provide overall constant gain.
-AHL I	-A HOLD IN	Port A Power Sequence Hold. See paragraph 4.13.15.
-AHL O	-A HOLD OUT	Port A Power Sequence Hold. See paragraph 4.13.15.
AIDX-N	A INDEX-NEG	Port A Reserved for Index pulse obtained from servo tracks. See paragraph 4.4.7.
AIDX-P	A INDEX-POS	Port A Reserved for Index pulse obtained from servo tracks. See paragraph 4.4.7.
+AM ACTIVE	+ADDRESS MARK ACTIVE	Prevents write data from going to write driver circuits.
-AM DETECTED	-ADDRESS MARK DETECTED	Active when AM detect circuit counts absence of 16 consecu- tive MFM data bits.
-AM ENABLE (-ADDRESS MARK ENABLE)	(SEE ADDRESS MARK ENABLE)	
-AM SEARCH	-ADDRESS MARK SEARCH	When active, this signal enables AM detection circuit. See paragraph 4.13.14.
+AM WRITE	+ADDRESS MARK WRITE	When active, this signal prevents the transfer of write data to the write drivers.
ANALOG A	ANALOG A	Automatic gain control dif- ference signals to read detector.

LOGIC TERMS (Cont.)

Term	Name	Function
ANALOG B	ANALOG B	Automatic gain control difference signals to read detector.
ARCK-N	A READ CLOCK-NEG	Port A Read Clock. See paragraph 4.4.1.
ARCK-P	A READ CLOCK-POS	Port A Read Clock. See paragraph 4.4.1.
ARDT-N	A READ DATA-NEG	Port A Read Data. See paragraph 4.4.2.
ARDT-P	A READ DATA-POS	Port A Read Data. See paragraph 4.4.2.
ARDV-N	A RECEIVE DEVICE-NEG	Port A Device Enable (Open Cable Detect). See paragraph 4.3.1.
ARDV-P	A RECEIVE DEVICE-POS	Port A Device Enable (Open Cable Detect). See paragraph 4.3.1.
ARSO-N	A RECEIVE SELECT 0-NEG	Port A Unit Select (2 ⁰). See paragraph 4.3.3.
ARSO-P	A RECEIVE SELECT 0-POS	Port A Unit Select (2 ⁰). See paragraph 4.3.3.
ARS1-N	A RECEIVE SELECT 1-NEG	Port A Unit Select (2 ¹). See paragraph 4.3.3.
ARS1-P	A RECEIVE SELECT 1-POS	Port A Unit Select (2 ¹). See paragraph 4.3.3.
ARS2-N	A RECEIVE SELECT 2-NEG	Port A Unit Select (2 ²). See paragraph 4.3.3.
ARS2-P	A RECEIVE SELECT 2-POS	Port A Unit Select (2 ²). See paragraph 4.3.3.
ARS3-N	A RECEIVE SELECT 3-NEG	Port A Unit Select (2 ³). See paragraph 4.3.3.
ARS3-P	A RECEIVE SELECT 3-POS	Port A Unit Select (2 ³). See paragraph 4.3.3.
ARSL-N	A RECEIVE SELECT-NEG	Port A Select Enable (Unit Select Tag). See paragraph 4.3.2.
ARSL-P	A RECEIVE SELECT-POS	Port A Select Enable (Unit Select Tag). See paragraph 4.3.2.

LOGIC TERMS (Cont.)

Term	Name	Function
VSCK-N	A SERVO CLOCK-NEG	Port A Servo Clock. See paragraph 4.4.5.
ASCK-P	A SERVO CLOCK-POS	Port A Servo Clock. See paragraph 4.4.5.
ASCT-N	A SECTOR-NEG	Port A Reserved for Sector pulse obtained from servo tracks. See paragraph 4.4.8.
ASCT-P	A SECTOR-POS	Port A Reserved for Sector pulse obtained from servo tracks. See paragraph 4.4.8.
ASEL-N	A SELECTED-NEG	Port A Unit Selected pulse indicates drive has accepted Unit Select request and must be active before drive responds to any CU command.
ASEL-P	A SELECTED-POS	Port A Unit Selected pulse indicates drive has accepted Unit Select request and must be active before drive responds to any CU command.
SKN-N	A SEEK END-NEG	Active at completion of carriage operation or seek incomplete condition. See paragraph 4.4.6.
ASKN-P	A SEEK END-POS	Active at completion of carriage operation or seek incomplete condition. See paragraph 4.4.6.
-ASQ I	-A SEQUENCE IN	Port A Power Sequence Pick. See paragraph 4.13.15.
-ASQ O	-A SEQUENCE OUT	Port A Power Sequence Pick. See paragraph 4.13.15.
AWCK-N	A WRITE CLOCK-NEG	Port A Write Clock. See paragraph 4.4.3.
AWCK-P	A WRITE CLOCK-POS	Port A Write Clock. See paragraph 4.4.3.
AWDT-N	A WRITE DATA-NEG	Port A Write Data. See paragraph 4.4.4.
AWDT-P	A WRITE DATA-POS	Port A Write Data. See paragraph 4.4.4.

LOGIC TERMS (Cont.)

Term	Name	Function
-B BUS 0	-B BUS 0	Enabled Bus Out 0 from Port B --Signal function determined by configuration of function-tag control lines. See paragraph 4.3.
-B BUS 1	-B BUS 1	Enabled Bus 1 from Port B --Signal function determined by configuration of function-tag control lines. See paragraph 4.3.
-B BUS 10	-B BUS 10	Enabled Bus 10 (9160 emulation) of Port B. See paragraph 4.3.6.
-B BUS 2	-B BUS 2	Enabled Bus 2 from Port B --Signal function determined by configuration of function-tag control lines. See paragraph 4.3.
-B BUS 3	-B BUS 3	Enabled Bus 3 from Port B --Signal function determined by configuration of function-tag control lines. See paragraph 4.3.
-B BUS 4	-B BUS 4	Enabled Bus 4 from Port B --Signal function determined by configuration of function-tag control lines. See paragraph 4.3.
-B BUS 5	-B BUS 5	Enabled Bus 5 from Port B --Signal function determined by configuration of function-tag control lines. See paragraph 4.3.
-B BUS 6	-B BUS 6	Enabled Bus 6 from Port B --Signal function determined by configuration of function-tag control lines. See paragraph 4.3.
-B BUS 7	-B BUS 7	Enabled Bus 7 from Port B --Signal function determined by configuration of function-tag control lines. See paragraph 4.3.

LOGIC TERMS (Cont.)

Term	Name	Function
B BUS 8	-B BUS 8	Enabled Bus 8 from Port B --Signal function determined by configuration of function-tag control lines. See paragraph 4.3.
-B BUS 9	-B BUS 9	Enabled Bus 9 from Port B --Signal function determined by configuration of function-tag control lines. See paragraph 4.3.
+B BUS 9	+B BUS 9	Enabled Bus 9 from Port B --Signal function determined by configuration of function-tag control lines. See paragraph 4.3.
-B CONTROL TAG	-B CONTROL TAG	Port B Control Select (Tag 3). See paragraph 4.3.6.
+B PORT ENABLE	+B PORT ENABLE	Signal generated by Port B Select Logic to enable some Port B transmitters.
-B PORT ENABLE	-B PORT ENABLE	Signal generated by Port B Select Logic to enable some Port B receivers.
-B PRIORITY	-B PRIORITY	Clears Port A 500 ms release timer flip-flop. Inhibits timer when priority selected by B Port.
-B RAW SELECT	-B RAW SELECT	Asynchronous Port B selected signal used to clock Port B priority logic.
-B RESERVED	-B RESERVED	Active when Port B is selected and/or reserved, providing Port A is not reserved.
+B RESERVED	+B RESERVED	Active when Port B is selected and/or reserved, providing Port A is not reserved.
+B SEEK END	+B SEEK END	Active at completion of carriage motion operation or seek incomplete condition. See paragraph 4.4.6.
B SELECT 0	-B SELECT 0	One of four binary coded unit selection lines. See paragraph 4.3.3.

LOGIC TERMS (Cont.)

Term	Name	Function
-B SELECT 1	-B SELECT 1	One of four binary coded unit selection lines. See paragraph 4.3.3.
-B SELECT 2	-B SELECT 2	One of four binary coded unit selection lines. See paragraph 4.3.3.
-B SELECT 3	-B SELECT 3	One of four binary coded unit selection lines. See paragraph 4.3.3.
-B SELECT ENABLE	-B SELECT ENABLE	When active, this signal permits binary decoding of Port B Device Select lines. See paragraph 4.3.2.
+B SELECTED	+B SELECTED	Used to enable one transmitter and is source signal for term BSEL-N and BSEL-P (selected status to controller).
-B SELECTED	-B SELECTED	Used as input to Reserve logic.
BB10-N	B BUS 10-NEG	Port B Bus Out 10 (DM9160). See paragraph 4.3.6.
BB10-P	B BUS 10-POS	Port B Bus Out 10 (DM9160). See paragraph 4.3.6.
BBS0-N	B BUS 0-NEG	Port B Bus Out 0 —Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS0-P	B BUS 0-POS	Port B Bus Out 0 —Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS1-N	B BUS 1-NEG	Port B Bus Out 1 —Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS1-P	B BUS 1-POS	Port B Bus Out 1 —Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.

LOGIC TERMS (Cont.)

Term	Name	Function
BS2-N	B BUS 2-NEG	Port B Bus Out 2 --Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS2-P	B BUS 2-POS	Port B Bus Out 2 --Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS3-N	B BUS 3-NEG	Port B Bus Out 3 --Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS3-P	B BUS 3-POS	Port B Bus Out 3 --Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS4-N	B BUS 4-NEG	Port B Bus Out 4 --Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS4-P	B BUS 4-POS	Port B Bus Out 4 --Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS5-N	B BUS 5-NEG	Port B Bus Out 5 --Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS5-P	B BUS 5-POS	Port B Bus Out 5 --Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS6-N	B BUS 6-NEG	Port B Bus Out 6 --Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.

LOGIC TERMS (Cont.)

Term	Name	Function
BBS6-P	B BUS 6-POS	Port B Bus Out 6 —Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS7-N	B BUS 7-NEG	Port B Bus Out 7 —Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS7-P	B BUS 7-POS	Port B Bus Out 7 —Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS8-N	B BUS 8-NEG	Port B Bus Out 8 —Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS8-P	B BUS 8-POS	Port B Bus Out 8 —Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS9-N	B BUS 9-NEG	Port B Bus Out 9 —Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BBS9-P	B BUS 9-POS	Port B Bus Out 9 —Signal function is determined by configuration of function-tag control lines. See paragraph 4.3.
BFT1-N	B FUNCTION TAG 1-NEG	Port B Cylinder Select (Tag 1). See paragraph 4.3.4.
BFT1-P	B FUNCTION TAG 1-POS	Port B Cylinder Select (Tag 1). See paragraph 4.3.4.
BFT2-N	B FUNCTION TAG 2-NEG	Port B Head Select (Tag 2). See paragraph 4.3.5.
BFT2-P	B FUNCTION TAG 2-POS	Port B Head Select (Tag 2). See paragraph 4.3.5.

LOGIC TERMS (Cont.)

Term	Name	Function
FT3-N	B FUNCTION TAG 3-NEG	Port B Control Select (Tag 3). See paragraph 4.3.6.
BFT3-P	B FUNCTION TAG 3-POS	Port B Control Select (Tag 3). See paragraph 4.3.6.
BHL1	B HOLD 1	Port B Power Sequence Hold. See paragraph 4.13.15.
BIDX-N	B INDEX-NEG	Port B Reserved for Index pulse obtained from servo tracks. See paragraph 4.4.7.
BIDX-P	B INDEX-POS	Port B Reserved for Index pulse obtained from servo tracks. See paragraph 4.4.7.
+BRAKE COIL	+BRAKE COIL	Pull-in and hold voltages for brake coil during Start and Run, respectively.
BRCK-N	B READ CLOCK-NEG	Port B Read Clock. See para- graph 4.4.1.
BRCK-P	B READ CLOCK-POS	Port B Read Clock. See para- graph 4.4.1.
BRDT-N	B READ DATA-NEG	Port B Read Data. See para- graph 4.4.2.
BRDT-P	B READ DATA-POS	Port B Read Data. See para- graph 4.4.2.
BRDV-N	B RECEIVE DEVICE-NEG	Port B Device Enable (Open Cable Detect). See paragraph 4.3.1.
BRDV-P	B RECEIVE DEVICE-POS	Port B Device Enable (Open Cable Detect). See paragraph 4.3.1.
BRS0-N	B RECEIVE SELECT 0-NEG	Port B Unit Select (2^0). See paragraph 4.3.3.
BRS0-P	B RECEIVE SELECT 0-POS	Port B Unit Select (2^0). See paragraph 4.3.3.
BRS1-N	B RECEIVE SELECT 1-NEG	Port B Unit Select (2^1). See paragraph 4.3.3.
BRS1-P	B RECEIVE SELECT 1-POS	Port B Unit Select (2^1). See paragraph 4.3.3.
BRS2-N	B RECEIVE SELECT 2-NEG	Port B Unit Select (2^2). See paragraph 4.3.3.

LOGIC TERMS (Cont.)

Term	Name	Function
BRS2-P	B RECEIVE SELECT 2-POS	Port B Unit Select (2 ²). See paragraph 4.3.3.
BRS3-N	B RECEIVE SELECT 3-NEG	Port B Unit Select (2 ³). See paragraph 4.3.3.
BRS3-P	B RECEIVE SELECT 3-POS	Port B Unit Select (2 ³). See paragraph 4.3.3.
BBSL-N	B RECEIVE SELECT-NEG	Port B Select Enable (Unit Select Tag). See paragraph 4.3.2.
BBSL-P	B RECEIVE SELECT-POS	Port B Select Enable (Unit Select Tag). See paragraph 4.3.2.
BSCK-N	B SERVO CLOCK-NEG	Port B Servo Clock. See paragraph 4.4.5.
BSCK-P	B SERVO CLOCK-POS	Port B Servo Clock. See paragraph 4.4.5.
BSCT-N	B SECTOR-NEG	Port B Reserved for Sector Pulse obtained from servo tracks. See paragraph 4.4.8.
BSCT-P	B SECTOR-POS	Port B Reserved for Sector Pulse obtained from servo tracks. See paragraph 4.4.8.
BSEL-N	B SELECTED-NEG	Port B Selected pulse, which indicates drive has accepted Unit Select request, must be active before drive responds to any CU command.
BSEL-P	B SELECTED-POS	Port B Selected pulse, which indicates drive has accepted Unit Select request, must be active before drive responds to any CU command.
BSKN-N	B SEEK END-NEG	Port B Seek End. See paragraph 4.4.6.
BSKN-P	B SEEK END-POS	Port B Seek End. See paragraph 4.4.6.
BSQ I	B SEQUENCE IN	Port B Power Sequence Pick. See paragraph 4.13.15.
-BSQ O	B SEQUENCE OUT	Port B Power Sequence Pick. See paragraph 4.13.15.

LOGIC TERMS (Cont.)

Term	Name	Function
3FT3-N	B FUNCTION TAG 3-NEG	Port B Control Select (Tag 3). See paragraph 4.3.6.
BFT3-P	B FUNCTION TAG 3-POS	Port B Control Select (Tag 3). See paragraph 4.3.6.
BHL1	B HOLD 1	Port B Power Sequence Hold. See paragraph 4.13.15.
BIDX-N	B INDEX-NEG	Port B Reserved for Index pulse obtained from servo tracks. See paragraph 4.4.7.
BIDX-P	B INDEX-POS	Port B Reserved for Index pulse obtained from servo tracks. See paragraph 4.4.7.
+BRAKE COIL	+BRAKE COIL	Pull-in and hold voltages for brake coil during Start and Run, respectively.
BRCK-N	B READ CLOCK-NEG	Port B Read Clock. See para- graph 4.4.1.
BRCK-P	B READ CLOCK-POS	Port B Read Clock. See para- graph 4.4.1.
BRDT-N	B READ DATA-NEG	Port B Read Data. See para- graph 4.4.2.
BRDT-P	B READ DATA-POS	Port B Read Data. See para- graph 4.4.2.
BRDV-N	B RECEIVE DEVICE-NEG	Port B Device Enable (Open Cable Detect). See paragraph 4.3.1.
BRDV-P	B RECEIVE DEVICE-POS	Port B Device Enable (Open Cable Detect). See paragraph 4.3.1.
BRS0-N	B RECEIVE SELECT 0-NEG	Port B Unit Select (2^0). See paragraph 4.3.3.
BRS0-P	B RECEIVE SELECT 0-POS	Port B Unit Select (2^0). See paragraph 4.3.3.
BRS1-N	B RECEIVE SELECT 1-NEG	Port B Unit Select (2^1). See paragraph 4.3.3.
BRS1-P	B RECEIVE SELECT 1-POS	Port B Unit Select (2^1). See paragraph 4.3.3.
BRS2-N	B RECEIVE SELECT 2-NEG	Port B Unit Select (2^2). See paragraph 4.3.3.

LOGIC TERMS (Cont.)

Term	Name	Function
3RS2-P	B RECEIVE SELECT 2-POS	Port B Unit Select (2 ²). See paragraph 4.3.3.
BRS3-N	B RECEIVE SELECT 3-NEG	Port B Unit Select (2 ³). See paragraph 4.3.3.
BRS3-P	B RECEIVE SELECT 3-POS	Port B Unit Select (2 ³). See paragraph 4.3.3.
BRSL-N	B RECEIVE SELECT-NEG	Port B Select Enable (Unit Select Tag). See paragraph 4.3.2.
BRSL-P	B RECEIVE SELECT-POS	Port B Select Enable (Unit Select Tag). See paragraph 4.3.2.
BSCK-N	B SERVO CLOCK-NEG	Port B Servo Clock. See paragraph 4.4.5.
BSCK-P	B SERVO CLOCK-POS	Port B Servo Clock. See paragraph 4.4.5.
BSCT-N	B SECTOR-NEG	Port B Reserved for Sector Pulse obtained from servo tracks. See paragraph 4.4.8.
BSCT-P	B SECTOR-POS	Port B Reserved for Sector Pulse obtained from servo tracks. See paragraph 4.4.8.
BSEL-N	B SELECTED-NEG	Port B Selected pulse, which indicates drive has accepted Unit Select request, must be active before drive responds to any CU command.
BSEL-P	B SELECTED-POS	Port B Selected pulse, which indicates drive has accepted Unit Select request, must be active before drive responds to any CU command.
BSKN-N	B SEEK END-NEG	Port B Seek End. See paragraph 4.4.6.
BSKN-P	B SEEK END-POS	Port B Seek End. See paragraph 4.4.6.
-BSQ I	B SEQUENCE IN	Port B Power Sequence Pick. See paragraph 4.13.15.
-BSQ O	B SEQUENCE OUT	Port B Power Sequence Pick. See paragraph 4.13.15.

LOGIC TERMS (Cont.)

Term	Name	Function
BUS 0	-BUS 0	ORed Bus Out 0 from Port A, Port B, or diagnostics. See paragraph 4.3.
+BUS 0	+BUS 0	ORed Bus Out 0 from Port A, Port B, or diagnostics. See paragraph 4.3.
-BUS 1	-BUS 1	ORed Bus Out 1 from Port A, Port B, or diagnostics. See paragraph 4.3.6.
+BUS 1	+BUS 1	ORed Bus Out 1 from Port A, Port B, or diagnostics. See paragraph 4.3.
-BUS 10	-BUS 10	ORed Bus Out 10 (9160E emulation) from Port A or Port B.
-BUS 2	-BUS 2	ORed Bus Out 2 from Port A, Port B, or diagnostics. See paragraph 4.3.
+BUS 2	+BUS 2	ORed Bus Out 2 from Port A, Port B, or diagnostics. See paragraph 4.3.
-BUS 3	-BUS 3	ORed Bus Out 3 from Port A, Port B, or diagnostics. See paragraph 4.3.
+BUS 3	+BUS 3	ORed Bus Out 3 from Port A, Port B, or diagnostics. See paragraph 4.3.
-BUS 4	-BUS 4	ORed Bus Out 4 from Port A or Port B. See paragraph 4.3.
+BUS 4	+BUS 4	ORed Bus Out 4 from Port A or Port B. See paragraph 4.3.
-BUS 5	-BUS 5	ORed Bus Out 5 from Port A, Port B, or diagnostics. See paragraph 4.3.
+BUS 5	+BUS 5	ORed Bus Out 5 from Port A, Port B, or diagnostics. See paragraph 4.3.
-BUS 6	-BUS 6	ORed Bus Out 6 from Port A or Port B. See paragraph 4.3.
BUS 6	BUS 6	ORed Bus Out 6 from Port A or Port B. See paragraph 4.3.

LOGIC TERMS (Cont.)

Term	Name	Function
BUS 7	-BUS 7	ORed Bus Out 7 from Port A or Port B. See paragraph 4.3.
+BUS 7	+BUS 7	ORed Bus Out 7 from Port A or Port B. See paragraph 4.3.
-BUS 8	-BUS 8	ORed Bus Out 8 from Port A or Port B.
+BUS 8	+BUS 8	ORed Bus Out 8 from Port A or Port B.
+BUS 9	+BUS 9	Generated by release logic when either -A Release or -B Release is true.
BWCK-G	B WRITE CLOCK-GND	Ground for Port B Write Clock. See paragraph 4.4.3.
BWCK-N	B WRITE CLOCK-NEG	Port B Write Clock. See paragraph 4.4.3.
BWCK-P	B WRITE CLOCK-POS	Port B Write Clock. See paragraph 4.4.3.
BWDT-G	B WRITE DATA-GND	Ground for Port B Write Data. See paragraph 4.4.4.
BWDT-N	B WRITE DATA-NEG	Port B Write Data. See paragraph 4.4.4.
BWDT-P	B WRITE DATA-POS	Port B Write Data. See paragraph 4.4.4.
+CAR 1	+CYLINDER ADDRESS REGISTER 1	One of two lower address bits that are decoded to determine proper quadrature input to produce position error code voltage.
+CAR 2	+CYLINDER ADDRESS REGISTER 2	One of two lower address bits that are decoded to determine proper quadrature input to produce position error code voltage.
-CEMH 0 (CHIP EN 0)	-CHIP ENABLE MAGNETIC HEAD 0	Selects read/write head arm 0.
-CEMH 1 (CHIP ENABLE 1)	-CHIP ENABLE MAGNETIC HEAD 1	Selects read/write head arm 1.
-CEMH 2 (CHIP ENABLE 2)	-CHIP ENABLE MAGNETIC HEAD 2	Selects read/write head arm 2.

LOGIC TERMS (Cont.)

Term	Name	Function
-CEMH 3 (CHIP ENABLE 3)	-CHIP ENABLE MAGNETIC HEAD 3	Selects read/write head arm :
-COLUMN X1	-COLUMN X1	Active when any SPST switch i column 1 of diagnostic panel is closed.
-COLUMN X2	-COLUMN X2	Active when any SPST switch i column 2 of diagnostic panel is closed.
-COLUMN X3	-COLUMN X3	Active when any SPST switch i column 3 of diagnostic panel is closed.
-COLUMN X4	-COLUMN X4	Active when any SPST switch i column 4 of diagnostic panel is closed.
-CONTROLLER RESET	-CONTROLLER RESET	When active, this signal resets Unsafe latch.
CYL TRANS	CYLINDER TRANS	Used to decrement the cylinder count as each cylinder is crossed. This signal display a TTL level transition for each cylinder crossed.
-CYLINDER TAG	-CYLINDER TAG	When active, strobes control logic to input cylinder address on I/O bus.
-D BUS 0	-DIAGNOSTIC BUS 0	Write gate and head address control signal internally generated by diagnostic logic.
-D BUS 1	-DIAGNOSTIC BUS 1	Read gate and head address control signal internally generated by diagnostics logic.
-D BUS 2	-DIAGNOSTIC BUS 2	Head Address control signal internally generated by diagnostics logic.
-D BUS 3	-DIAGNOSTIC BUS 3	Head Address signal internal generated by diagnostics logic.
-D BUS 5	-DIAGNOSTIC BUS 5	Address Mark control signal internally generated by diagnostics logic.
-D CONTROL TAG	-DIAGNOSTIC CONTROL TAG	Active after detection of index and enables function gates during diagnostics.

LOGIC TERMS (Cont.)

Term	Name	Function
+D1SA	+DISPLAY DIGIT 1, SEGMENT A	Drives respective element of display A4DS1.
+D1SB	+DISPLAY DIGIT 1, SEGMENT B	Drives respective element of display A4DS1.
+D1SC	+DISPLAY DIGIT 1, SEGMENT C	Drives respective element of display A4DS1.
+D1SD	+DISPLAY DIGIT 1, SEGMENT D	Drives respective element of display A4DS1.
+D1SE	+DISPLAY DIGIT 1, SEGMENT E	Drives respective element of display A4DS1.
+D1SF	+DISPLAY DIGIT 1, SEGMENT F	Drives respective element of display A4DS1.
+D1SG	+DISPLAY DIGIT 1, SEGMENT G	Drives respective element of display A4DS1.
+D2SA	+DISPLAY DIGIT 2, SEGMENT A	Drives respective element of display A4DS2.
+D2SB	+DISPLAY DIGIT 2, SEGMENT B	Drives respective element of display A4DS2.
+D2SC	+DISPLAY DIGIT 2, SEGMENT C	Drives respective element of display A4DS2.
+D2SD	+DISPLAY DIGIT 2, SEGMENT D	Drives respective element of display A4DS2.
+D2SE	+DISPLAY DIGIT 2, SEGMENT E	Drives respective element of display A4DS2.
+D2SF	+DISPLAY DIGIT 2, SEGMENT F	Drives respective element of display A4DS2.
+D2SG	+DISPLAY DIGIT 2, SEGMENT G	Drives respective element of display A4DS2.
+D3SA	+DISPLAY DIGIT 3, SEGMENT A	Drives respective element of display A4DS3.
+D3SB	+DISPLAY DIGIT 3, SEGMENT B	Drives respective element of display A4DS3.
+D3SC	+DISPLAY DIGIT 3, SEGMENT C	Drives respective element of display A4DS3.
+D3SD	+DISPLAY DIGIT 3, SEGMENT D	Drives respective element of display A4DS3.

LOGIC TERMS (Cont.)

Term	Name	Function
+D3SE	+DISPLAY DIGIT 3, SEGMENT E	Drives respective element of display A4DS3.
+D3SF	+DISPLAY DIGIT 3, SEGMENT F	Drives respective element of display A4DS3.
+D3SG	+DISPLAY DIGIT 3, SEGMENT G	Drives respective element of display A4DS3.
+D4SA	+DISPLAY DIGIT 4, SEGMENT A	Drives respective element of display A4DS4.
+D4SB	+DISPLAY DIGIT 4, SEGMENT B	Drives respective element of display A4DS4.
+D4SC	+DISPLAY DIGIT 4, SEGMENT C	Drives respective element of display A4DS4.
+D4SD	+DISPLAY DIGIT 4, SEGMENT D	Drives respective element of display A4DS4.
+D4SE	+DISPLAY DIGIT 4, SEGMENT E	Drives respective element of display A4DS4.
+D4SF	+DISPLAY DIGIT 4, SEGMENT F	Drives respective element of display A4DS4.
+D4SG	+DISPLAY DIGIT 4, SEGMENT G	Drives respective element of display A4DS4.
+DATA AVAILABLE	+DATA AVAILABLE	This signal is active when the keyboard data is latched within the decode circuit and output of decode circuit is valid.
+DATA HOLD	+DATA HOLD	Enable signal for read data.
+DHAR 1	+DIAGNOSTIC HEAD ADDRESS REGISTER 1	One bit (2 ⁰) of binary coded address for one of 16 data heads. Head address ranges from 00 to 15 for Model 330, 00 to 09 for Model 165, and 0 to 04 for model 165E. This bit is generated internally for diagnostic operations.
+DHAR 2	+DIAGNOSTIC HEAD ADDRESS REGISTER 2	One bit (2 ¹) of binary coded address for one of 16 data heads. Head address ranges from 00 to 15 for Model 330, 00 to 09 for Model 165, and 0 to 04 for model 165E. This bit is generated internally for diagnostic operations.

LOGIC TERMS (Cont.)

Term	Name	Function
+DHAR 4	+DIAGNOSTIC HEAD ADDRESS REGISTER 4	One bit (2 ²) of binary coded address for one of 16 data heads. Head address ranges from 00 to 15 for Model 330, 00 to 09 for Model 165, and 00 to 04 for model 165E. This bit is generated internally for diagnostic operations.
+DHAR 8	+DIAGNOSTIC HEAD ADDRESS REGISTER 8	One bit (2 ³) of binary coded address for one of 16 data heads. Head address ranges from 00 to 15 for Model 330, 00 to 09 for Model 165, and 00 to 04 for model 165E. This bit is generated internally for diagnostic operations.
-DIAGNOSTIC (DIAGNOSTIC SWITCH)	DIAGNOSTIC	Enables diagnostic mode when DIAG/NORMAL switch (A4S1) is set to DIAG position.
-DIAGNOSTICS	DIAGNOSTICS	Enables diagnostic mode when DIAG/NORMAL switch (A4S1) is set to DIAG position.
-DIAGNOSTICS TEST	DIAGNOSTIC TEST	Active when operating system is in diagnostic mode.
-DIFF 1 (-1)	-DIFFERENCE 1	Data from difference counter used as input to the desired velocity profile generator to represent the magnitude of the difference between the current cylinder and the destination cylinder before the completion of seek.
-DIFF 1024 (-1024)	-DIFFERENCE 1024	Not Used
-DIFF 128 (-128)	-DIFFERENCE 128	Data from difference counter used as input to the desired velocity profile generator to represent the magnitude of the difference between the current cylinder and the destination cylinder before the completion of seek.

LOGIC TERMS (Cont.)

Term	Name	Function
-DIFF 16 (-16)	-DIFFERENCE 16	Data from difference counter used as input to the desired velocity profile generator to represent the magnitude of the difference between the current cylinder and the destination cylinder before the completion of seek.
-DIFF 2 (-2)	-DIFFERENCE 2	Data from difference counter used as input to the desired velocity profile generator to represent the magnitude of the difference between the current cylinder and the destination cylinder before the completion of seek.
-DIFF 256 (-256)	-DIFFERENCE 256	Not Used
->DIFF 256 (->256)	-EQUAL TO OR GREATER THAN DIFF. 256	Data from difference counter used as input to the desired velocity profile generator to represent the magnitude of the difference between the current cylinder and the destination cylinder before the completion of seek.
-DIFF 32 (-32)	-DIFFERENCE 32	Data from difference counter used as input to the desired velocity profile generator to represent the magnitude of the difference between the current cylinder and the destination cylinder before the completion of seek.
-DIFF 4 (-4)	-DIFFERENCE 4	Data from difference counter used as input to the desired velocity profile generator to represent the magnitude of the difference between the current cylinder and the destination cylinder before the completion of seek.
-DIFF 512 (-512)	-DIFFERENCE 512	Data from difference counter used as input to the desired velocity profile generator to represent the magnitude of the difference between the current cylinder and the destination cylinder before the completion of seek.

LOGIC TERMS (Cont.)

Term	Name	Function												
-DIFF 64 (-64)	-DIFFERENCE 64	Data from difference counter used as input to the desired velocity profile generator to represent the magnitude of the difference between the current cylinder and the destination cylinder before the completion of seek.												
-DIFF 8 (-8)	-DIFFERENCE 8	Data from difference counter used as input to the desired velocity profile generator to represent the magnitude of the difference between the current cylinder and the destination cylinder before the completion of seek.												
+DIFF <>0	+DIFFERENCE LESS THAN OR MORE THAN 0	Output from difference counter that is used to determine the positioning mode.												
-DIFF <>0	-DIFFERENCE LESS THAN OR MORE THAN 0	Output from difference counter that is used with LOCK ON to determine the positioning mode. Truth table for position mode selection is:												
		-DIFF<>0 -LOCK ON MODE <table> <tr> <td>0</td><td>0</td><td>PES Position Error Signal</td></tr> <tr> <td>0</td><td>1</td><td>TACH-A - DESIRED VELOCITY</td></tr> <tr> <td>1</td><td>0</td><td>PES (fine mode)</td></tr> <tr> <td>1</td><td>1</td><td>PES + TACH-A</td></tr> </table>	0	0	PES Position Error Signal	0	1	TACH-A - DESIRED VELOCITY	1	0	PES (fine mode)	1	1	PES + TACH-A
0	0	PES Position Error Signal												
0	1	TACH-A - DESIRED VELOCITY												
1	0	PES (fine mode)												
1	1	PES + TACH-A												
-DIFF CLOCK	-DIFFERENCE CLOCK	Use to increment difference counter.												
-DISABLE A	-DISABLE PORT A	Used to disable Port A during diagnostics or when Port B is reserved.												
-DISABLE B	-DISABLE PORT B	Used to disable Port B during diagnostics or when Port A is reserved.												

LOGIC TERMS (Cont.)

Term	Name	Function
+EN SEQ TNU	+ENABLE SEQUENCE TO NEXT UNIT	This signal, which becomes active when the drive is up to speed, deenergizes the sequence relay which permits sequence pick signal (ASQ0) to be sent to next drive.
-ERROR 1	-ERROR 1	Represents bit 2 ⁰ of binary decoded error for micro-processor to display.
-ERROR 2	-ERROR 2	Represents bit 2 ¹ of binary decoded error for micro-processor to display.
-ERROR 4	-ERROR 4	Represents bit 2 ² of binary decoded error for micro-processor to display.
ERROR AMP	ERROR AMPLIFIER	Amplified tachometer position error signal.
-FAULT RESET SW	FAULT RESET SWITCH	Resets unsafe latch A1U76 when switch A4S2 is momentarily closed.
+FEEDBACK PULSE TTL	+FEEDBACK PULSE TRANSISTOR-TO- TRANSISTOR LOGIC	PLO feedback compare signal to phase detector.
+FILE READY	+FILE READY	This signal is active when disk is up to speed, heads are located over data track and no fault condition exists.
-FINE TRACK	-FINE TRACK	Used to verify accurate carriage position during data transfers (delimits the area nearest to track center for writing). Once the carriage is in the fine position (tracking following) mode, the -FINE TRACK signal will be low while the carriage stays within 78 microinches of the track. This signal is bandwidth limited and will not be dependable during the high velocity period of long seek.
-GATE 1	-GATE 1	This signal gates -SERVO BIT signal to A3C93 for peak detection during seeks and on track conditions.

LOGIC TERMS (Cont.)

Term	Name	Function
-GATE 2	-GATE 2	This signal gates -SERVO BITS signal to A3C94 for peak detection during seeks and on-track conditions.
-GATE 3	-GATE 3	This signal gates -SERVO BITS signal to A3C95 for peak detection during seeks and on-track conditions.
-GATE 4	-GATE 4	This signal gates -SERVO BITS signal to A3C96 for peak detection during seeks and on-track conditions.
-GATED MULT HD (-MULTI CHIP SEL)	-GATED MULTIPLE HEAD	This signal is active when more than one head is selected at the same time.
-GATED R/W UNSAFE (-R/W UNSAFE)	-GATED READ/WRITE UNSAFE	This signal is active if MARS Unsafe is true from 10 milliseconds after leading edge of Write Gate until 10 milliseconds after trailing edge of Write Gate; held inactive during Address Mark.
-GATED WRITE	-GATED WRITE	Active when all write requirements are valid.
+GATED WS	+GATED WRITE SELECT	Used to generate Write Select which enables SSI-104 chips in HDA.
-GATED WS	-GATED WRITE SELECT	Used to generate Write Select which enables SSI-104 chips in HDA.
+GB ERROR	+GUARD BAND ERROR	Active when heads drift into guardband area.
-H VEL	-HIGH VELOCITY	Output of tachometer comparators; used to determine current through sample-and-hold circuit of servo peak detector.
-HAR 1	HEAD ADDRESS REGISTER BIT 1	One bit (2 ⁰) of binary coded address for one of 16 data heads. Head address ranges from 00 to 15 for Model 330, 00 to 09 for Model 165, and 0 to 04 for model 165E.

LOGIC TERMS (Cont.)

Term	Name	Function
-HAR 2	HEAD ADDRESS REGISTER BIT 2	One bit (2 ¹) of binary coded address for one of 16 data heads. Head address ranges from 00 to 15 for Model 330, 00 to 09 for Model 165, and 0 to 04 for model 165E.
-HAR 4	HEAD ADDRESS REGISTER BIT 4	One bit (2 ²) of binary coded address for one of 16 data heads. Head address ranges from 00 to 15 for Model 330, 00 to 09 for Model 165, and 0 to 04 for model 165E.
-HAR 8	HEAD ADDRESS REGISTER BIT 8	One bit (2 ³) of binary coded address for one of 16 data heads. Head address ranges from 00 to 15 for Model 330, 00 to 09 for Model 165, and 0 to 04 for model 165E.
-HEAD TAG (-HD TAG)	-HEAD TAG	Head Select control signal. See paragraph 4.3.5.
+HOLD	+HOLD	Active until address mark is detected during a read address mark operation; inhibits Read Gate.
-HS1 (-HEAD SELECT 1)	-HEAD SELECT 1	One of two address signals that are binary encoded to select one of four heads.
-HS2 (-HEAD SELECT 2)	-HEAD SELECT 2	One of two address signals that are binary encoded to select one of four heads.
I/O BUS	INPUT/OUTPUT BUS	Input/Output lines of the Z80 microprocessor.
+INDEX	+INDEX	When active, indicates reference point or index area is passing under the servo head.
+INDEX BYTE TTL	+INDEX BYTE TRANSISTOR- TO-TRANSISTOR	Used to load PLO locked/unlocked detector and to generate Servo One Byte.
-INDEX ENABLE	-INDEX ENABLE	Active once every revolution of the cylinder counter; sets index latch and loads sector pulse generator.

LOGIC TERMS (Cont.)

Term	Name	Function
+INDEX FOUND	+INDEX FOUND	Active when Index is in sync with read/write gate generator of diagnostics logic.
+INDEX GATE (+INDEX GATE TTL)	+INDEX GATE	Used to detect sync pulse in servo data which determines index position.
-INDEX RESET	-INDEX RESET	When active, this signal resets index latch and inhibits guard band decoder.
-INITIALIZE	-INITIALIZE	Resets head address selector register.
-INTERRUPT	-INTERRUPT	Maskable interrupt to microprocessor; generated by ORED outputs of rezero and seek latches.
+INWARD	+INWARD	Used during power-up diagnostics to verify +24V power supply is correct.
-IP10	-INPUT PORT 10	Enables input port flip-flops of microprocessor bus logic.
-IP11	-INPUT PORT 11	Enables input port flip-flops of microprocessor bus logic.
-IP12	-INPUT PORT 12	Enables input port flip-flops of microprocessor bus logic.
-IP13	-INPUT PORT 13	Enables input port flip-flops of microprocessor bus logic.
-IP14	-INPUT PORT 14	Enables input port flip-flops of microprocessor bus logic.
-IP15	-INPUT PORT 15	Enables input port flip-flops of microprocessor bus logic.
-IP16	-INPUT PORT 16	Enables input port flip-flops of microprocessor bus logic.
-IP17	-INPUT PORT 17	Enables input port flip-flops of microprocessor bus logic.
+KEY 1	+KEY 1	One bit (2 ⁰) of four binary outputs of keyboard decode logic that represents selected diagnostic function.

LOGIC TERMS (Cont.)

Term	Name	Function
+KEY 2	+KEY 2	One bit (2 ¹) of four binary outputs of keyboard decode logic that represents selected diagnostic function.
+KEY 4	+KEY 4	One bit (2 ²) of four binary outputs of keyboard decode logic that represents selected diagnostic function.
+KEY 8	+KEY 8	One bit (2 ³) of four binary outputs of keyboard decode logic that represents selected diagnostic function.
-LOCK ON	-LOCK ON	This signal is active when the servo is on track.
-M VEL (-MED VEL)	-MEDIUM VELOCITY	Output of tachometer comparators; used to determine current through sample-and-hold circuit of servo peak detector.
MARS UNSAFE	MULTIPLE ADDRESS REGISTER SELECT UNSAFE	Active when more than one head is addressed, current unsafe, or write transitions error.
+MCS (+MSC)	+MULTI CHIP SELECT	Sets Unsafe latch when more than one chip is selected.
-MODULE 1	-MODULE 1	One of four binary coded HDA identification bits (2 ⁰) that identify the HDA as Model 165, 165E, or 330.
-MODULE 2	-MODULE 2	One of four binary coded HDA identification bits (2 ¹) that identify the HDA as Model 165, 165E, or 330.
-MODULE 4	-MODULE 4	One of four binary coded HDA identification bits (2 ²) that identify the HDA as Model 165, 165E, or 330.
-MODULE 8	-MODULE 8	One of four binary coded HDA identification bits (2 ³) that identify the HDA as Model 165, 165E, or 330.
MOTOR DRIVE	MOTOR DRIVE	Power line that supplies current to run linear motor. (Same as MOTOR HI)

LOGIC TERMS (Cont.)

Term	Name	Function
MOTOR HI	MOTOR HIGH	Power line that supplies current to run linear motor. (Same as MOTOR DRIVE)
-MOVE OUT	-MOVE OUT	Polarity of this signal determines whether the heads move toward or away from the spindle.
+MOVE OUT	+MOVE OUT	Polarity of this signal determines whether the heads move toward or away from the spindle.
MTR I FDBK	MOTOR I FEEDBACK (Current Sense)	Motor feedback to comparator circuit of tachometer for servo correction.
NP	NORMAL POSITION	Signal NP is one of the track servo position signals used to generate the cylinder pulse.
NP XING	NORMAL POSITION CROSSING	Not Used.
+ODD HEAD	+ODD HEAD	Firmware generated signal that indicates odd or even head for 9160 emulation.
-OFFSET	-OFFSET	Active when the read/write heads are to be positioned off track; the carriage moves 60 microinches off-track in the direction specified by the -MOVE OUT signal.
+OFFSET FORWARD	+OFFSET FORWARD	When active, this signal causes head positioner to move 60 microinches toward spindle from on-track position.
+OFFSET REVERSE	+OFFSET REVERSE	When active, this signal causes head positioner to move 60 microinches away from spindle from on-track position.
-OFFSET SELECT	-OFFSET SELECT	Active when either forward or reverse offset is selected; an input to Write Error Encoder, which in turn generates binary octal output.

LOGIC TERMS (Cont.)

Term	Name	Function
+OGB #1	+OUTER GUARD BAND NO. 1	Active when servo decoder selects 011000 because heads are over outer guardband 1, which is located outside of normal recording track area; used to rezero.
OGB #2	OUTER GUARD BAND NO. 2	Active when servo decoder selects 011011 because heads are over outer guardband 2, which is located outside of normal recording track area; used to rezero.
+ON CYLINDER	+ON CYLINDER	Active when servo has positioned head over selected cylinder.
+ON TRACK	+ON TRACK	This signal is gated with - INTERRUPT (FALSE) to generate +ON CYLINDER.
-OP20	-OUTPUT PORT 20	Clocks I/O bus data through output port flip-flops of microprocessor bus logic.
-OP21	-OUTPUT PORT 21	Clocks I/O bus data through output port flip-flops of microprocessor bus logic.
-OP22	-OUTPUT PORT 22	Clocks I/O bus data through output port flip-flops of microprocessor bus logic.
-OP23	-OUTPUT PORT 23	Loads difference counter.
-OP24	-OUTPUT PORT 24	Loads difference counter.
-OP25	-OUTPUT PORT 25	Enables display drivers.
-OP26	-OUTPUT PORT 26	Enables display drivers.
-OP40	-OUTPUT PORT 40	Clocks serial shift-bit register of the pseudo-random data generator for internal diagnostics.
-OP41	-OUTPUT PORT 41	Clocks serial shift-bit register of the pseudo-random data generator for internal diagnostics.

LOGIC TERMS (Cont.)

Term	Name	Function
-OP42	-OUTPUT PORT 42	Clocks serial shift-bit register of the pseudo-random data generator for internal diagnostics.
-OP43	-OUTPUT PORT 43	Clocks sync-field register for diagnostic write pattern.
-OP44	-OUTPUT PORT 44	Clocks read/write gate generation flip-flops.
-OP45	-OUTPUT PORT 45	Generates term HEAD TAG for diagnostics and enables head-select gates for diagnostics.
-OPEN CABLE DETECT	-OPEN CABLE DETECT	Active when cable is disconnected; unit selection and/or CU commands consequently are inhibited.
+OPEN CABLE DETECT	+OPEN CABLE DETECT	Active when cable is disconnected; unit selection and/or CU commands consequently are inhibited.
-OUTER TRACK	-OUTER TRACK	Active when head is located between cylinders 0 to 511; used to determine write current switching.
OUTPUT +(SERVO-X)	OUTPUT +	Servo head signal from servo preamplifier.
OUTPUT -(SERVO-Y)	OUTPUT -	Servo head signal from servo preamplifier.
+OUTWARD	+OUWARD	Used during power-up diagnostics to determine -24V power supply is correct.
-PLO	-PHASE LOCK OSCILLATOR	PLO output (9.67 MHz) used as source for fanout signal 9.67 CLOCK BUF 1.
+PLO LOCKED TTL	+PHASE LOCK OSCILLATOR LOCKED TRANSISTOR- TO-TRANSISTOR LOGIC	Active when PLO is locked.

LOGIC TERMS (Cont.)

Term	Name	Function
+PLO UNSAFE TTL (+PLO UNSAFE)	+PHASE LOCK OSCILLATOR UNSAFE TRANSISTOR- TO-TRANSISTOR LOGIC	The +PLO UNSAFE will be at a logic "1" state whenever more than three consecutive servo bytes without a sync pulse (S2) are detected. This signal is reset to logic "0" when more than 15 consecutive servo bytes with a sync pulse are detected.
+PLO UNSAFE (+PLO UNSAFE TTL)	+PHASE LOCK OSCILLATOR UNSAFE TRANSISTOR- TO-TRANSISTOR LOGIC	The +PLO UNSAFE will be at a logic "1" state whenever more than three consecutive servo bytes without a sync pulse (S2) are detected. This signal is reset to logic "0" when more than 15 consecutive servo bytes with a sync pulse are detected.
POWER ON RESET	POWER ON RESET	Active with power up and presence of +5V regulated voltage; forces CPU program counter to zero and initializes CPU.
-PWR FAIL (-POWER FAIL)	-POWER FAIL	Active when drive power fails; causes a non-maskable interrupt of CPU.
QP	QUADRATURE POSITION	Signal QP is one of the track servo position signals used to generate the cylinder pulse.
+QP XING	+QUATRATURE POSITION CROSSING	(See term QP) NOT USED
+R/W UNSAFE	+READ/WRITE UNSAFE	This signal is active when a MARS unsafe condition exists.
-RAW READ DATA	-RAW READ DATA	This pulse (one for every zero crossing) clocks read generator and decoder.
+RAW READ DATA	+RAW READ DATA	This pulse (one for every zero crossing) clocks read generator and decoder.
+RD ERROR	+READ ERROR	Active when missing read bit is detected.
-RD ONLY LED (-READ ONLY LED)	-READ ONLY HIGH EMITTING DIODE	Drives READ ONLY LED (A4DS8) when switch A4S3 is in Read Only position.

LOGIC TERMS (Cont.)

Term	Name	Function
+READ	+READ	Used to sync read data buffer output.
-READ CLOCK	-READ CLOCK	Provides timing to allow sampling of clocked read data which appears on data line. See paragraph 4.4.1.
-READ CLOCK BUF 1	-READ CLOCK BUFFER 1	Provides timing to allow sampling of clocked read data which appears on data line. See paragraph 4.4.1.
-READ CLOCK BUF 2 (-CLOCK)	-READ CLOCK BUFFER 2	Provides timing to allow sampling of clocked read data which appears on data line. See paragraph 4.4.1.
-READ DATA	-READ DATA	Read Data. See paragraph 4.4.2.
-READ DATA BUF 1	-READ DATA BUFFER 1	Read Data. See paragraph 4.4.2.
-READ DATA BUF 2 (-DATA)	-READ DATA BUFFER 2	Read Data. See paragraph 4.4.2.
-READ GATE	-READ GATE	Used to control phase lock loop.
+READ GATE (+RD GATE)	+READ GATE	Used to control phase lock loop.
-READ ONLY SW	-READ ONLY SWITCH	Disables drive from performing a write operation when READ ONLY switch (A4S3) is in Read position.
+READY	+READY	Active when disk is up to speed and heads are located over a data track.
-READY LED	-READY LIGHT EMITTING DIODE	Drives A4DS6 when drive is on-line, spindle is up to speed and heads are positioned.
-RESET	-RESET	On power-up, resets AM, read/write, and read error logics.
-RESET GB ERROR	-RESET GUARD BAND ERROR	Resets guard band error latch.
-RESET INTERRUPT	-RESET INTERRUPT	Active when operation is completed to set rezero, off-set and seek interrupt latches.
-RESET UNSAFE	-RESET UNSAFE	Resets unsafe latch.

LOGIC TERMS (Cont.)

Term	Name	Function
+PLO UNSAFE TTL (+PLO UNSAFE)	+PHASE LOCK OSCILLATOR UNSAFE TRANSISTOR- TO-TRANSISTOR LOGIC	The +PLO UNSAFE will be at a logic "1" state whenever more than three consecutive servo bytes without a sync pulse (S ₂) are detected. This signal is reset to logic "0" when more than 15 consecutive servo bytes with a sync pulse are detected.
+PLO UNSAFE (+PLO UNSAFE TTL)	+PHASE LOCK OSCILLATOR UNSAFE TRANSISTOR- TO-TRANSISTOR LOGIC	The +PLO UNSAFE will be at a logic "1" state whenever more than three consecutive servo bytes without a sync pulse (S ₂) are detected. This signal is reset to logic "0" when more than 15 consecutive servo bytes with a sync pulse are detected.
POWER ON RESET	POWER ON RESET	Active with power up and presence of +5V regulated voltage; forces CPU program counter to zero and initializes CPU.
-PWR FAIL (-POWER FAIL)	-POWER FAIL	Active when drive power fails; causes a non-maskable interrupt of CPU.
QP	QUADRATURE POSITION	Signal QP is one of the track servo position signals used to generate the cylinder pulse.
+QP XING	+QUATRATURE POSITION CROSSING	(See term QP) NOT USED
+R/W UNSAFE	+READ/WRITE UNSAFE	This signal is active when a MARS unsafe condition exists.
-RAW READ DATA	-RAW READ DATA	This pulse (one for every zero crossing) clocks read generator and decoder.
+RAW READ DATA	+RAW READ DATA	This pulse (one for every zero crossing) clocks read generator and decoder.
+RD ERROR	+READ ERROR	Active when missing read bit is detected.
-RD ONLY LED (-READ ONLY LED)	-READ ONLY HIGH EMITTING DIODE	Drives READ ONLY LED (A4DS8) when switch A4S3 is in Read Only position.

LOGIC TERMS (Cont.)

Term	Name	Function
+READ	+READ	Used to sync read data buffer output.
-READ CLOCK	-READ CLOCK	Provides timing to allow sampling of clocked read data which appears on data line. See paragraph 4.4.1.
-READ CLOCK BUF 1	-READ CLOCK BUFFER 1	Provides timing to allow sampling of clocked read data which appears on data line. See paragraph 4.4.1.
-READ CLOCK BUF 2 (-CLOCK)	-READ CLOCK BUFFER 2	Provides timing to allow sampling of clocked read data which appears on data line. See paragraph 4.4.1.
-READ DATA	-READ DATA	Read Data. See paragraph 4.4.2.
-READ DATA BUF 1	-READ DATA BUFFER 1	Read Data. See paragraph 4.4.2.
-READ DATA BUF 2 (-DATA)	-READ DATA BUFFER 2	Read Data. See paragraph 4.4.2.
-READ GATE	-READ GATE	Used to control phase lock loop.
+READ GATE (+RD GATE)	+READ GATE	Used to control phase lock loop.
-READ ONLY SW	-READ ONLY SWITCH	Disables drive from performing a write operation when READ ONLY switch (A4S3) is in Read position.
+READY	+READY	Active when disk is up to speed and heads are located over a data track.
-READY LED	-READY LIGHT EMITTING DIODE	Drives A4DS6 when drive is on-line, spindle is up to speed and heads are positioned.
-RESET	-RESET	On power-up, resets AM, read/write, and read error logics.
-RESET GB ERROR	-RESET GUARD BAND ERROR	Resets guard band error latch.
-RESET INTERRUPT	-RESET INTERRUPT	Active when operation is completed to set rezero, offset and seek interrupt latches.
-RESET UNSAFE	-RESET UNSAFE	Resets unsafe latch.

LOGIC TERMS (Cont.)

Term	Name	Function
-REZERO	-REZERO	When active, starts rezero operation; the carriage moves away from the spindle at 6 in/sec until the second outer guardband is detected, then turns around and approaches track zero at 2.5 in/sec through the first guardband.
+REZERO INT	-REZERO INTERRUPT	Active at start of operation.
-ROW Y1	-ROW Y1	Active when any SPST switch in row 1 of diagnostic control panel is closed.
-ROW Y2	-ROW Y2	Active when any SPST switch in row 2 of diagnostic control panel is closed.
-ROW Y3	-ROW Y3	Active when any SPST switch in row 3 of diagnostic control panel is closed.
-ROW Y4	-ROW Y4	Active when any SPST switch in row 4 of diagnostic control panel is closed.
+RUN	+RUN	When active, removes Reset on servo pattern shift register and enables servo power amplifier.
-RUN	-RUN	When active, removes Reset on servo pattern shift register and enables servo power amplifier.
-RUN RELAY DRIVE	-RUN RELAY DRIVE	When active, drives solid state RUN relays.
+SECTOR PULSE	+SECTOR PULSE	Active when sector pulse generator has counted pulses equal to programmed sector capacity.
+SEEK INCOMPLETE	+SEEK INCOMPLETE	Becomes active from unsuccessful termination of initial head load or of normal seek command. See paragraph 4.3.10
+SEEK INT	+SEEK INTERRUPT	Becomes active from seek incomplete and Cylinder Tag active.

LOGIC TERMS (Cont.)

Term	Name	Function
-SELECT LED (SELECT LED)	-SELECTED LIGHT EMITTING DIODE	Drives indicator A4DS5 when drive is selected by control unit.
-SELECT SW0	-SELECT SWITCH 0	Drive select switch with value 2 ⁰ . See paragraph 3.2.2.2.
-SELECT SW1	-SELECT SWITCH 1	Drive select switch with value 2 ¹ . See paragraph 3.2.2.2.
-SELECT SW2	-SELECT SWITCH 2	Drive select switch with value 2 ² . See paragraph 3.2.2.2.
-SELECT SW3	-SELECT SWITCH 3	Drive select switch with value 2 ³ . See paragraph 3.2.2.2.
-SEQUENCE HOLD	-SEQUENCE HOLD	Power sequencing signal. See paragraph 4.3.15.
-SEQUENCE PICK	-SEQUENCE PICK	Power sequencing signal. See paragraph 4.3.15.
-SERVO BITS	-SERVO BITS	Amplified servo track signals; input to peak detectors.
-SERVO CLOCK TTL (+SERVO CLOCK)	-SERVO CLOCK TRANSISTOR-TO- TRANSISTOR LOGIC	Derived from IF VCO signal (9.67 MHz); used for synchron- izing data to actual speed of disk.
+SERVO CLOCK TTL (+SERVO CLOCK)	+SERVO CLOCK TRANSISTOR-TO- TRANSISTOR LOGIC	Derived from IF VCO signal (9.67 MHz); used for synchron- izing data to actual speed of disk.
-SERVO DISABLE	-SERVO DISABLE	Active during diagnostics to disable servo.

LOGIC TERMS (Cont.)

Term	Name	Function
SERVO ONE BYTE (SERVO ONE BYTE TTL)	SERVO ONE BYTE	The +SERVO ONE BYTE signal is at logic "1" whenever a missing S1 pulse is detected in the analog servo signal read from the servo surface. Any byte containing the S1 pulse is referred to as a servo "zero" byte. This distinction allows for the encoding of different guardbands and an index in the pre-written servo data on the servo surface of the pack. The following list describes the servo byte codes used for each guardband (GB) and the index: Inner GB: 011000 Outer GB1: 111001 Outer GB2: 011011 Index: 101010
SERVO ONE BYTE TTL (+SERVO ONE BYTE)	SERVO ONE BYTE TRANSISTOR-TO- TRANSISTOR LOGIC	The +SERVO ONE BYTE signal is at logic "1" whenever a missing S1 pulse is detected in the analog servo signal read from the servo surface. Any byte containing the S1 pulse is referred to as a servo "zero" byte. This distinction allows for the encoding of different guardbands and an index in the pre-written servo data on the servo surface of the pack. The following list describes the servo byte codes used for each guardband (GB) and the index: Inner GB: 011000 Outer GB1: 111001 Outer GB2: 011011 Index: 101010
SERVO VOLTAGE	SERVO VOLTAGE	This signal is used by the I/O and Control PWBA to perform a test on the servo driver during the power-up sequence for the disk drive. With the linear VCM coil switched out of the circuit, the power driver is exercised and the output voltage checked to verify that the servo PWBA functions properly.

LOGIC TERMS (Cont.)

Term	Name	Function
-SET UNSAFE	-SET UNSAFE	When active, sets Unsafe latch.
+SPLIT FIELD	+SPLIT FIELD	Active, except when emulating DM9160; input to HAR multiplexer.
SQUARED SERVO BITS	SQUARED SERVO BITS	Amplified and squared servo bits from special detector digitizer (these signals are TTL representations of the analog servo signals being read from the servo surface).
-SQUARED SERVO BITS (-SERVO SQUARE BITS)	-SQUARED SERVO BITS	Amplified and squared servo bits from special detector digitizer (these signals are TTL representations of the analog servo signals being read from the servo surface).
-START	-START	When active, drives start relay of power supply.
-START RELAY DRIVE	-START RELAY DRIVE	When active, drives start relay of power supply.
-STROBE EARLY	-STROBE EARLY	Data strobe early. See paragraph 4.3.6.
-STROBE LATE	-STROBE LATE	Data strobe late. See paragraph 4.3.6.
-SYNC BYTE TTL	-SYNC BYTE TRANSISTOR- TO-TRANSISTOR LOGIC	Loads PLO locked/unlocked detector.
+SYNC ERROR	+SYNC ERROR	Active when Read Data is out of sync with read gate.
+SYNC FOUND	+SYNC FOUND	Active when Sync Byte TTL is true with read gate.
+SYNC GATE TTL	+SYNC GATE TRANSISTOR- TO-TRANSISTOR LOGIC	Enables Sync Byte latch.
TABY-N	TRANSMIT A BUSY-NEG	Port A Busy Status. See paragraph 4.5.3.
TABY-P	TRANSMIT A BUSY-POS	Port A Busy Status. See paragraph 4.5.3.

LOGIC TERMS (Cont.)

Term	Name	Function
TACH-A	TACHOMETER A	Output of electronic tachometer; input to the comparators which determine high or medium velocity and to the comparator which determines (servo) error amplifier output.
TACY-N	TRANSMIT A CYLINDER-NEG	Port A On Cylinder Status. See paragraph 4.3.11.
TACY-P	TRANSMIT A CYLINDER-POS	Port A On Cylinder Status. See paragraph 4.3.11.
TAFT-N	TRANSMIT A FAULT-NEG	Port A Fault (Read/Write Unsafe). See paragraph 4.3.9
TAFT-P	TRANSMIT A FAULT-POS	Port A Fault (Read/Write Unsafe). See paragraph 4.3.9
TAIN-N	TRANSMIT A INDEX-NEG	Port A Index. See paragraph 4.3.7.
TAIN-P	TRANSMIT A INDEX-POS	Port A Index. See paragraph 4.3.7.
TAMK-N	TRANSMIT A MARK-NEG	Port A Address Mark Found. See paragraph 4.3.14.
TAMK-P	TRANSMIT A MARK-POS	Port A Address Mark Found. See paragraph 4.3.14.
TARD-N	TRANSMIT A READY-NEG	Port A Unit Ready. See paragraph 4.3.12.
TARD-P	TRANSMIT A READY-POS	Port A Unit Ready. See paragraph 4.3.12.
TASC-N	TRANSMIT A SECTOR-NEG	Port A Sector Mark. See paragraph 4.3.8.
TASC-P	TRANSMIT A SECTOR-POS	Port A Sector Mark. See paragraph 4.3.8.
TASE-N	TRANSMIT A SEEK ERROR-NEG	Port A Seek Error. See paragraph 4.3.10.
TASE-P	TRANSMIT A SEEK ERROR-POS	Port A Seek Error. See paragraph 4.3.10.
TAWP-N	TRANSMIT A WRITE PROTECT-NEG	Port A Write Protected. See paragraph 4.3.13.
TAWP-P	TRANSMIT A WRITE PROTECT-POS	Port A Write Protected. See paragraph 4.3.13.

LOGIC TERMS (Cont.)

Term	Name	Function
TBBY-N	TRANSMIT B BUSY-NEG	Port B Busy Status. See paragraph 4.5.3.
TBBY-P	TRANSMIT B BUSY-POS	Port B Busy Status. See paragraph 4.5.3.
TBCK-N	TRANSMIT B CYLINDER-NEG	Port B On Cylinder Status. See paragraph 4.3.11.
TBCK-P	TRANSMIT B CYLINDER-POS	Port B On Cylinder Status. See paragraph 4.3.11.
TBFT-N	TRANSMIT B FAULT-NEG	Port B Fault (Read/Write Unsafe). See paragraph 4.3.9.
TBFT-P	TRANSMIT B FAULT-POS	Port B Fault (Read/Write Unsafe). See paragraph 4.3.9.
TBIN-N	TRANSMIT B INDEX-NEG	Port B Index. See paragraph 4.3.7.
TBIN-P	TRANSMIT B INDEX-POS	Port B Index. See paragraph 4.3.7.
TBMK-N	TRANSMIT B MARK-NEG	Port B Address Mark Found. See paragraph 4.3.14.
TBMK-P	TRANSMIT B MARK-POS	Port B Address Mark Found. See paragraph 4.3.14.
TBRD-N	TRANSMIT B READY-NEG	Port B Ready. See paragraph 4.3.12.
TBRD-P	TRANSMIT B READY-POS	Port B Ready. See paragraph 4.3.12.
TBSC-N	TRANSMIT B SECTOR-NEG	Port B Sector Mark. See paragraph 4.3.8.
TBSC-P	TRANSMIT B SECTOR-POS	Port B Sector Mark. See paragraph 4.3.8.
TBSE-N	TRANSMIT B SEEK ERROR-NEG	Port B Seek Error. See paragraph 4.3.10.
TBSE-P	TRANSMIT B SEEK ERROR-POS	Port B Seek Error. See paragraph 4.3.10.
TBWP-N	TRANSMIT B WRITE PROTECT-NEG	Port B Write Protected. See paragraph 4.3.13.
TBWP-P	TRANSMIT B WRITE PROTECT-POS	Port B write Protected. See paragraph 4.3.13.

LOGIC TERMS (Cont.)

Term	Name	Function
THRESHOLD	THRESHOLD	Compensates AGC when address mark is active (no data pulses are present during this time).
-UNSAFE	-UNSAFE	Active when any unsafe condition exists within the drive.
+UNSAFE	+UNSAFE	Active when any unsafe condition exists within the drive.
+UNSAFE CLOCK	+UNSAFE CLOCK	Active when Unsafe is true and all reset conditions are false.
-UNSAFE LED (-FAULT LED)	UNSAFE LIGHT EMITTING DIODE	Drives A4DS7 when unsafe condition exists within drive.
+UPSPEED	+UPSPEED	Active when spindle reaches 78% of full speed.
VELCOMP1	VELOCITY COMPENSATOR 1	Outward movement compensator for desired velocity for 256 tracks or more to go.
VELCOMP2	VELOCITY COMPENSATOR 2	Inward and Outward movement compensator for desired velocity for 256 tracks or more to go.
VFO TO (+VCO TO)	VFO TIMEOUT	Output of 8-bit counter that is clocked by Read Clock, used to generate Head Sync Enable.
+WRITE	+WRITE	ANDed output of Index Found and Write Gate.
-WRITE CLOCK	-WRITE CLOCK	Used to synchronize write data. See paragraph 4.4.3.
-WRITE CLOCK BUF (-WRITE CLK)	-WRITE CLOCK BUFFER	ORed external and internal generated Write Clocks.
WRITE CURRENT	WRITE CURRENT	Write Current to heads; current defined by odd or even head and outer track.
-WRITE DATA	-WRITE DATA	Write data signals from CU. See paragraph 4.4.4.
-WRITE DATA BUF	-WRITE DATA BUFFER	ORed external and internal generated Write Data.

LOGIC TERMS (Cont.)

Term	Name	Function
-WRITE ERROR	-WRITE ERROR	Active when any of the following terms are active: PLO Unsafe, Read Gate, Read Only SW, Offset Select, or Fine Track.
-WRITE GATE	-WRITE GATE	When active, enables write drivers and write current.
+WRITE MFM	+WRITE MODIFIED FREQUENCY MODULATION	Output of NRZ to MFM conversion circuit.
-WRITE MFM	-WRITE MODIFIED FREQUENCY MODULATION	Output of NRZ to MFM conversion circuit.
+WRITE PATTERN	+WRITE PATTERN	Clocks serial shift-bit register with prescribed number of zeros loaded in write pattern generator (255).
+WRITE PROTECT	+WRITE PROTECT	Active when Read Only Switch is active.
WRITE SELECT (+WRITE SELECT)	WRITE SELECT	Write Select with chip enable generates Write Enable in pre-amplifier logic.

LOGIC TERMS

This section includes an alpha-numeric list of all logic terms for the Capricorn disk drive. The intent of this list is to assist the user in locating the source and destinations of logic signals. Moreover, this list is intended for reference use only and is not intended to be used as a wire list. In some cases, identical terms are given different term names. In these cases, the alternate term name is also listed in parenthesis. See Figure 1.

NOTE

The origin(s) of each signal is denoted by an asterisk (*).

Capricorn assembly designations are as follows:

- A1 -- I/O Control PCBA (CTROL)
- A2 -- Read/Write PCBA (READW)
- A3 -- Servo Driver PCBA (SERDV)
- A4 -- Diagnostic Control PCBA (DICO2)
- A5 -- Dual Port PCBA (DUPOC)
- A6 -- Power Supply Regulator PCBA (REGUL)
- A7 -- HDA Interface PCBA (HDAIN)

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
+ RAW READ DATA	A2U36-07	3310210	5A8
+ RAW READ DATA	A2U41-06	3310210	3C7
- RAW READ DATA	A2U56-10*	3310210	1C4
+ RAW READ DATA	A2U56-11*	3310210	1C4
+ RD ERROR	A1U98-09*	3309780	11C2
+ RD GATE (+READ GATE)	A2U38-05	3310210	2B2
+ RD GATE (+READ GATE)	A2U44-06	3310210	2B7
- RD ONLY LED (-READ ONLY LED)	A1J8-39	3309780	12A4
- RD ONLY LED (-READ ONLY LED)	A1U114-12*	3309780	10B1

ALPHA-NUMERIC TERM

SYMBOL INDICATES POLARITY OF SIGNAL WHEN ASSERTED (ABSENCE OF SIGN INDICATES POSITIVE POLARITY)

IDENTICAL SIGNAL WITH ALTERNATE TERM NAME (SEE ALTERNATE TERM NAME FOR REMAINING SIGNAL DESTINATION(S) OR ORIGIN(S).

PCBA

COMPONENT

PIN

INDICATES SIGNAL ORIGIN

SCHEMATIC DRAWING NO.

COORDINATES

SHEET NO. OF DRAWING

Figure 1

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-1 (-DIFF 1)	A3J3-34	3309770	6D8
-1 (-DIFF 1)	A3U13-02	3309770	6D7
-1/2T	A3U13-01	3309770	6D7
-1/2T	A3U24-11*	3309770	5D3
-128 (-DIFF 128)	A3J3-27	3309770	6C8
-128 (-DIFF 128)	A3U13-19	3309770	6C7
-16 (-DIFF 16)	A3J3-32	3309770	6D8
-16 (-DIFF 16)	A3U13-16	3309770	6D7
+1F	A3U70-03,11	3309770	3B4
+1F	A3U71-12*	3309770	2B1
+1F	A3U74-03,11	3309770	3C4
+1F	A3U78-03,11	3309770	3D4
+1F	A3U79-02	3309770	3C6
+1F	A3U82-03	3309770	3C7
+1F	A3U82-11	3309770	3B4
-2 (-DIFF 2)	A3J3-33	3309770	6D8
-2 (-DIFF 2)	A3U13-03	3309770	6D7
2 FPLO -(2 FPLO +2)	A2U31-03*	3309760	3C7
2 FPLO -(2 FPLO +2)	A2U29-05	3309760	3C6
2 FPLO -(2 FPLO +2)	A2U41-11	3309760	3C7
+2F (+2 FS)	A3U10-01*	3309770	2C1
+2F (+2 FS)	A3J1-01	3309770	2C1
-2F (-2 FS)	A3J1-02	3309770	2C1
-2F (-2 FS)	A3U10-02*	3309770	2C1
2F PLO	A2U16-11	3309760	2C5
2F PLO	A2U36-02	3309760	3C8
2F PLO	A2U31-06	3309760	3C7
2F PLO	A2U26-15*	3309760	2C7
2F PLO+2	A2U45-06	3309760	5C7
2F PLO+2	A2U36-03	3309760	5C7
+2FS (+2F)	A2U26-13	3309760	2C7
+2FS (+2F)	A2J3-01	3309760	2C7
-2FS (-2F)	A2J3-02	3309760	2C8
-2FS (-2F)	A2U26-12	3309760	2C7
-32 (-DIFF 32)	A3U13-17	3309770	6D7
-32 (-DIFF 32)	A3J3-30	3309770	6D8
-4 (-DIFF 4)	A3U13-04	3309770	6D7
-4 (-DIFF 4)	A3J3-31	3309770	6D8
-4 MHZ CLOCK	A5U24-05	3316180	5B7
-4 MHZ CLOCK	A5U4-11	3316180	5B3
-4 MHZ CLOCK	A1J4-32	3309780	12B2
-4 MHZ CLOCK	A1U16-04*	3309780	4C4
-4 MHZ CLOCK	A1U17-05	3309780	4B5
-4 MHZ CLOCK	A1U26-11	3309780	4D4
-4 MHZ CLOCK	A5J4-32	3316180	1C7
+4 MHZ CLOCK	A1U16-03	3309780	4C4
+4 MHZ CLOCK	A1U87-11	3309780	7A7
+4 MHZ CLOCK	A1U64-11	3309780	7C6
+4 MHZ CLOCK	A1U35-02*	3309780	6C7
+4 MHZ CLOCK	A1U86-11	3309780	7D6
+4 MHZ CLOCK	A1U119-11	3309780	7B6
+4 MHZ CLOCK	A1U97-11	3309780	11C1

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-512 (-DIFF 512)	A3U1-01	3309770	6C5
-512 (-DIFF 512)	A3J3-08	3309770	6C8
-64 (-DIFF 64)	A3J3-28	3309770	6C8
-64 (-DIFF 64)	A3U13-18	3309770	6C7
+6V R/W CHIP	A2VR3*	3309760	2B7
+6V R/W CHIP	A2J2-23	3309760	2B1
-8 (-DIFF 8)	A3J3-29	3309770	6D8
-8 (-DIFF 8)	A3U13-05	3309770	6D7
-9.67 CLOC BUF 2	A5J4-07	3316180	1C7
+9.67 CLOCK	A1U109-10	3309780	1C6
+9.67 CLOCK	A1U107-11	3309780	11B3
+9.67 CLOCK	A1U109-02	3309780	11B7
+9.67 CLOCK	A1U22-10	3309780	11A7
+9.67 CLOCK	A1U74-08*	3309780	11C7
+9.67 CLOCK	A1U95-05	3309780	11B1
-9.67 CLOCK BUF 1	A1U40-02	3309780	3D5
-9.67 CLOCK BUF 1	A1U40-03*	3309780	3D5
-9.67 CLOCK BUF 1	A1U95-13	3309780	9C8
-9.67 CLOCK BUF 1	A1U27-03	3309780	8C7
-9.67 CLOCK BUF 1	A1U74-09	3309780	11C8
-9.67 CLOCK BUF 2	A5U31-06	3316180	4C3
-9.67 CLOCK BUF 2 (-9.67 CLK)	A1J4-07	3309780	12D2
-9.67 CLOCK BUF 2 (-9.67 CLK)	A1U40-18*	3309780	3D4
->256 (-> DIFF 256)	A3U24-04	3309770	6C7
->256 (-> DIFF 256)	A3J3-13	3309770	6C8
-A BUS 9	A1U6-11*	3309780	1A5
-A BUS 9	A1U16-11	3309780	4B5
-A BUS 9	A1J4-23	3309780	12B2
-A BUS 9	A5U27-13	3316180	5D7
-A BUS 9	A5J4-23	3316180	1C7
-A CONTROL TAG	A1RP1-03	3309780	2B2
-A CONTROL TAG	A1RP1-03	3309780	2B1
-A CONTROL TAG	A1U11-13*	3309780	2B2
-A CONTROL TAG	A1J4-10	3309780	12C2
-A CONTROL TAG	A5U23-02	3316180	5C7
-A CONTROL TAG	A5J4-10	3316180	1C7
-A CONTROL TAG	A1U18-03	3309780	5C8
-A INHIBIT	A5J4-34	3316180	1B7
-A INHIBIT	A5U25-01*	3316180	5B2
-A INHIBIT	A1U17-12	3309780	4B6
-A INHIBIT	A1RP15-03	3309780	4B7
-A INHIBIT	A1J4-34	3309780	12C2
+A OR B SELECTED	A1U15-03*	3309780	4C3
+A OR B SELECTED	A1U114-01	3309780	10B2
+A PORT ENABLE	A1U7-06	3309780	3C8
+A PORT ENABLE	A1U18-12*	3309780	4D3
+A PORT ENABLE	A1U8-06	3309780	3A8
-A PORT ENABLE	A1U37-03*	3309780	4D3
-A PORT ENABLE	A1U4-04	3309780	2A7
-A PORT ENABLE	A1U11-04	3309780	2A3
-A PRIORITY	A5U21-08*	3316180	5D4
-A PRIORITY	A5U26-01	3316180	5A6

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-A RAW SELECT	A1J4-33	3309780	12B2
-A RAW SELECT	A1U26-06*	3309780	4C5
-A RAW SELECT	A5U12-02	3316180	5A7
-A RAW SELECT	A5J4-33	3316180	1C7
-A RAW SELECT	A5U2-09	3316180	5C6
-A RAW SELECT	A5U10-05	3316180	5D6
-A RAW SELECT	A5U27-05	3316180	5C5
-A RELEASE	A5U23-01	3316180	5C7
-A RELEASE	A5J4-25	3316180	1C7
-A RELEASE	A1U15-13	3309780	4B4
-A RELEASE	A1U15-06*	3309780	4B4
-A RELEASE	A1J4-25	3309780	12B2
+A RESERVED	A5U10-01	3316180	5C7
+A RESERVED	A5U31-01	3316180	4D3
+A RESERVED	A5U12-01	3316180	5A7
+A RESERVED	A5U7-02	3316180	5A4
+A RESERVED	A5U25-05	3316180	5A3
+A RESERVED	A5U10-13	3316180	5C2
+A RESERVED	A5U19-05*	3316180	5C2
+A RESERVED	A5U4-02	3316180	5D3
+A RESERVED	A5J4-26	3316180	1C7
+A RESERVED	A1J4-26	3309780	12C2
+A RESERVED	A1RP15-06	3309780	4C7
+A RESERVED	A1U15-04	3309780	4B5
+A RESERVED	A1U18-13	3309780	4C3
+A SEEK END	A1U12-15	3309780	3B3
+A SEEK END	A1U25-01	3309780	4B3
-A SELECT 0	A1U2-11*	3309780	1D5
-A SELECT 1	A1U2-13*	3309780	1C5
-A SELECT 2	A1U2-05*	3309780	1C5
-A SELECT 3	A1U2-03*	3309780	1C5
-A SELECT ENABLE	A1U35-12*	3309780	1B5
-A SELECT ENABLE	A1U37-13	3309780	4D6
-A SELECT ENABLE	A1U35-03	3309780	4C6
-A SELECTED	A5U12-10	3316180	5D4
-A SELECTED	A5J4-28	3316180	1C7
-A SELECTED	A5U24-03	3316180	5D5
-A SELECTED	A1U15-01	3309780	4C3
-A SELECTED	A1J4-28	3309780	12B2
-A SELECTED	A1U26-08*	3309780	4C3
+A SELECTED	A1U12-10	3309780	3B3
+A SELECTED	A1U18-02	3309780	4D3
+A SELECTED	A1U21-03	3309780	3D3
+A SELECTED	A1U26-09*	3309780	4C3
AB10-N	A1RP5-05	3309780	2D3
AB10-P	A1RP5-07	3309780	2D3
ABS0-N	A1RP7-05	3309780	2D7
ABS0-N	A1J2-04	3309780	2D8
ABS0-N	A1J1-04*	3309780	2D8
ABS0-P	A1J1-34*	3309780	2D8
ABS0-P	A1J2-34	3309780	2D8
ABS0-P	A1RP7-07	3309780	2D7

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
ABS1-N	A1RP7-04	3309780	2D7
ABS1-N	A1J1-05*	3309780	2D8
ABS1-N	A1J2-05	3309780	2D8
ABS1-P	A1J1-35*	3309780	2D8
ABS1-P	A1J2-35	3309780	2D8
ABS1-P	A1RP7-01	3309780	2D7
ABS10-N	A1J1-30*	3309780	2D4
ABS10-N	A1J2-30	3309780	2D4
ABS10-P	A1J2-60	3309780	2D4
ABS10-P	A1J1-60*	3309780	2D4
ABS2-N	A1J2-06	3309780	2C8
ABS2-N	A1J1-06*	3309780	2C8
ABS2-N	A1RP8-04	3309780	2D7
ABS2-P	A1RP8-01	3309780	2D7
ABS2-P	A1J1-36*	3309780	2C8
ABS2-P	A1J2-36	3309780	2C8
ABS3-N	A1J2-07	3309780	2C8
ABS3-N	A1J1-07*	3309780	2C8
ABS3-N	A1RP8-07	3309780	2D7
ABS3-P	A1RP8-05	3309780	2D7
ABS3-P	A1J1-37*	3309780	2C8
ABS3-P	A1J2-37	3309780	2C8
ABS4-N	A1J2-08	3309780	2B8
ABS4-N	A1J1-08*	3309780	2B8
ABS4-N	A1RP9-05	3309780	2B7
ABS4-P	A1RP9-07	3309780	2B7
ABS4-P	A1J1-38*	3309780	2B8
ABS4-P	A1J2-38	3309780	2B8
ABS5-N	A1J2-09	3309780	2B8
ABS5-N	A1J1-09*	3309780	2B8
ABS5-N	A1RP9-04	3309780	2B7
ABS5-P	A1RP-01	3309780	2B7
ABS5-P	A1J1-39*	3309780	2B8
ABS5-P	A1J2-39	3309780	2B8
ABS6-N	A1J2-10	3309780	2B8
ABS6-N	A1J1-10*	3309780	2B8
ABS6-N	A1RP10-04	3309780	2B7
ABS6-P	A1J1-40*	3309780	2B8
ABS6-P	A1J2-40	3309780	2B8
ABS6-P	A1RP10-01	3309780	2B7
ABS7-N	A1RP10-07	3309780	2B7
ABS7-N	A1J2-11	3309780	2B8
ABS7-N	A1J1-11*	3309780	2B8
ABS7-P	A1J1-41*	3309780	2A8
ABS7-P	A1J2-41	3309780	2B8
ABS7-P	A1RP10-05	3309780	2B7
ABS8-N	A1RP5-04	3309780	2D3
ABS8-N	A1J2-12	3309780	2D4
ABS8-N	A1J1-12*	3309780	2D4
ABS8-P	A1J1-42*	3309780	2D4
ABS8-P	A1J2-42	3309780	2D4
ABS8-P	A1RP5-02	3309780	2D3

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
ABS9-N	A1U6-10	3309780	1A6
ABS9-N	A1J1-13*	3309780	1A8
ABS9-N	A1J2-13	3309780	1A7
ABS9-P	A1J1-43*	3309780	1A8
ABS9-P	A1J2-43	3309780	1A7
ABS9-P	A1U6-09	3309780	1A6
-ADDRESS MARK ENABLE (-AM ENABLE)	A1U33-11*	3309780	5B6
AFT1-N	A1RP6-04	3309780	2C3
AFT1-N	A1J2-01	3309780	2C4
AFT1-N	A1J1-01*	3309780	2C4
AFT1-P	A1J1-31*	3309780	2C4
AFT1-P	A1J2-31	3309780	2C4
AFT1-P	A1RP6-01	3309780	2C3
AFT2-N	A1RP6-07	3309780	2C3
AFT2-N	A1J2-02	3309780	2C4
AFT2-N	A1J1-02*	3309780	2C4
AFT2-P	A1J1-32*	3309780	2C4
AFT2-P	A1J2-32	3309780	2C4
AFT2-P	A1RP6-05	3309780	2C3
AFT3-N	A1U11-14	3309780	2B3
AFT3-N	A1J2-03	3309780	2B4
AFT3-N	A1J1-03*	3309780	2B4
AFT3-P	A1J1-33*	3309780	2B4
AFT3-P	A1J2-33	3309780	2B4
AFT3-P	A1U11-15	3309780	2B3
AGC	A3U75-01*	3309770	4C3
AGC	A3CR26	3309770	1D8
-AHL 0	A1J2-59	3309780	4A1
-AHL 1	A1U29-07	3309780	4B6
-AHL 1	A1J1-59*	3309780	4A8
AIDX-N	A1U12-03*	3309780	3B2
AIDX-N	A1J3-12	3309780	3B2
AIDX-P	A1J3-24	3309780	3A2
AIDX-P	A1U12-02*	3309780	3A2
+AM ACTIVE	A1U110-02	3309780	11B7
+AM ACTIVE	A1U106-05*	3309780	11B3
+AM ACTIVE	A1U97-04	3309780	11C1
AM DETECTED	A1J6-17	3309780	12C5
-AM DETECTED	A1J4-40	3309780	12C2
-AM DETECTED	A1U111-02	3309780	11C4
-AM DETECTED	A5J4-40	3316180	1B7
-AM DETECTED	A5U6-10	3316180	4B7
-AM DETECTED	A1U8-15	3309780	3B8
-AM DETECTED	A2U5-04*	3309760	5C2
-AM DETECTED	A2J1-17	3309760	5C2
-AM ENABLE (-ADDRESS MARK ENABLE)	A2U49-11	3309760	1B8
-AM ENABLE (-ADDRESS MARK ENABLE)	A2U43-05	3309760	3B7
-AM ENABLE (-ADDRESS MARK ENABLE)	A2Q6B	3309760	4D2
-AM ENABLE (-ADDRESS MARK ENABLE)	A2J1-09	3309760	3B7
-AM ENABLE (-ADDRESS MARK ENABLE)	A2U62-08	3309760	4D3
-AM ENABLE (-ADDRESS MARK ENABLE)	A1J6-09	3309780	12C5

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-AM SEARCH	A2U43-02*	3309760	3B7
-AM SEARCH	A2U47-13	3309760	5B7
+AM WRITE	A2U32-06	3309760	2C3
+AM WRITE	A2U38-07	3309760	2C2
+AM WRITE	A2U43-04*	3309760	3B7
ANALOG A	A2U69-07*	3309760	4D4
ANALOG A	A2U53-12	3309760	1C7
ANALOG A	A2U52-09	3309760	1D7
ANALOG B	A2U69-08*	3309760	4D4
ANALOG B	A2U53-11	3309760	1C7
ANALOG B	A2U52-10	3309760	1D7
ARCK-G	A1J3-04	3309780	3B2
ARCK-N	A1J3-05	3309780	3B2
ARCK-N	A1U21-13*	3309780	3C2
ARCK-P	A1U21-12*	3309780	3C2
ARCK-P	A1J3-17	3309780	3B2
ARDT-G	A1J3-15	3309780	3C2
ARDT-N	A1J3-03	3309780	3C3
ARDT-N	A1U21-08*	3309780	3C3
ARDT-P	A1U21-09*	3309780	3C2
ARDT-P	A1J3-16	3309780	3C2
ARDV-N	A1J2-14	3309780	1C7
ARDV-N	A1U6-14	3309780	1B6
ARDV-N	A1J1-14*	3309780	1C8
ARDV-P	A1U6-15	3309780	1B6
ARDV-P	A1J1-44*	3309780	1B8
ARDV-P	A1J2-44	3309780	1B7
ARSO-N	A1J2-23	3309780	1D7
ARSO-N	A1J1-23*	3309780	1D8
ARSO-N	A1U2-10	3309780	1D6
ARSO-P	A1J1-53*	3309780	1D8
ARSO-P	A1U2-09	3309780	1D6
ARSO-P	A1J2-53	3309780	1D7
ARS1-N	A1J2-24	3309780	1D7
ARS1-N	A1J1-24*	3309780	1D8
ARS1-N	A1U2-14	3309780	1D6
ARS1-P	A1U2-15	3309780	1C6
ARS1-P	A1J1-54*	3309780	1C8
ARS1-P	A1J2-54	3309780	1C7
ARS2-N	A1J2-26	3309780	1C7
ARS2-N	A1J1-26*	3309780	1C8
ARS2-N	A1U2-06	3309780	1C6
ARS2-P	A1U2-07	3309780	1C6
ARS2-P	A1J1-56*	3309780	1C8
ARS2-P	A1J2-56	3309780	1C7
ARS3-N	A1J2-27	3309780	1C7
ARS3-N	A1J1-27*	3309780	1C8
ARS3-N	A1U2-02	3309780	1C6
ARS3-P	A1U2-01	3309780	1C6
ARS3-P	A1J1-57*	3309780	1C8
ARS3-P	A1J2-57	3309780	1C7

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
ARSL-N	A1J2-22	3309780	1B7
ARSL-N	A1J1-22*	3309780	1B8
ARSL-N	A1U6-02	3309780	1B6
ARSL-P	A1U6-01	3309780	1B6
ARSL-P	A1J1-52*	3309780	1A8
ARSL-P	A1J2-52	3309780	1A7
ASCK-G	A1J3-01	3309780	3C2
ASCK-N	A1J3-02	3309780	3C2
ASCK-N	A1U20-08*	3309780	3C2
ASCK-P	A1U20-09*	3309780	3C2
ASCK-P	A1J3-14	3309780	3C2
ASCT-N	A1J3-13	3309780	3A2
ASCT-N	A1U12-04*	3309780	3A2
ASCT-P	A1U12-05*	3309780	3A2
ASCT-P	A1J3-26	3309780	3A2
ASEL-N	A1J3-22	3309780	3B2
ASEL-N	A1U12-12*	3309780	3B2
ASEL-P	A1U12-11*	3309780	3B2
ASEL-P	A1J3-09	3309780	3B2
ASKN-N	A1J3-10	3309780	3B2
ASKN-N	A1U12-13*	3309780	3B2
ASKN-P	A1U12-14*	3309780	3B2
ASKN-P	A1J3-23	3309780	3B2
-ASQ 0	A1J2-29	3309780	4A1
-ASQ 1	A1J1-29*	3309780	4A8
AWCK-G	A1J3-18	3309780	2A4
AWCK-N	A1J3-06*	3309780	2A4
AWCK-N	A1RP13-06	3309780	2A4
AWCK-P	A1RP13-19	3309780	2A4
AWCK-P	A1J3-19*	3309780	2A4
AWDT-G	A1J3-07	3309780	2B4
AWDT-N	A1J3-08*	3309780	2B4
AWDT-N	A1RP13-04	3309780	2B4
AWDT-P	A1J3-20*	3309780	2B4
AWDT-P	A1RP13-02	3309780	2B4
-B BUS 0	A5J4-16	3316180	1C7
-B BUS 0	A5U13-13*	3316180	3D6
-B BUS 0	A1J4-16	3309780	12D2
-B BUS 0	A1RP-02	3309780	2D6
-B BUS 1	A1J4-15	3309780	12D2
-B BUS 1	A1RP-08	3309780	2D6
-B BUS 1	A5J4-15	3316180	1C7
-B BUS 1	A5U13-11*	3316180	3C6
-B BUS 10	A5J4-12	3316180	1C7
-B BUS 10	A5U29-13*	3316180	3C2
-B BUS 10	A1RP1-04	3309780	2D2
-B BUS 10	A1J4-12	3309780	12C2
-B BUS 2	A1RP-03	3309780	2C6
-B BUS 2	A1J4-17	3309780	12D2
-B BUS 2	A5J4-17	3316180	1C7
-B BUS 2	A5U13-05*	3316180	3C6

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-AM SEARCH	A2U43-02*	3309760	3B7
-AM SEARCH	A2U47-13	3309760	5B7
+AM WRITE	A2U32-06	3309760	2C3
+AM WRITE	A2U38-07	3309760	2C2
+AM WRITE	A2U43-04*	3309760	3B7
ANALOG A	A2U69-07*	3309760	4D4
ANALOG A	A2U53-12	3309760	1C7
ANALOG A	A2U52-09	3309760	1D7
ANALOG B	A2U69-08*	3309760	4D4
ANALOG B	A2U53-11	3309760	1C7
ANALOG B	A2U52-10	3309760	1D7
ARCK-G	A1J3-04	3309780	3B2
ARCK-N	A1J3-05	3309780	3B2
ARCK-N	A1U21-13*	3309780	3C2
ARCK-P	A1U21-12*	3309780	3C2
ARCK-P	A1J3-17	3309780	3B2
ARDT-G	A1J3-15	3309780	3C2
ARDT-N	A1J3-03	3309780	3C3
ARDT-N	A1U21-08*	3309780	3C3
ARDT-P	A1U21-09*	3309780	3C2
ARDT-P	A1J3-16	3309780	3C2
ARDV-N	A1J2-14	3309780	1C7
ARDV-N	A1U6-14	3309780	1B6
ARDV-N	A1J1-14*	3309780	1C8
ARDV-P	A1U6-15	3309780	1B6
ARDV-P	A1J1-44*	3309780	1B8
ARDV-P	A1J2-44	3309780	1B7
ARSO-N	A1J2-23	3309780	1D7
ARSO-N	A1J1-23*	3309780	1D8
ARSO-N	A1U2-10	3309780	1D6
ARSO-P	A1J1-53*	3309780	1D8
ARSO-P	A1U2-09	3309780	1D6
ARSO-P	A1J2-53	3309780	1D7
ARS1-N	A1J2-24	3309780	1D7
ARS1-N	A1J1-24*	3309780	1D8
ARS1-N	A1U2-14	3309780	1D6
ARS1-P	A1U2-15	3309780	1C6
ARS1-P	A1J1-54*	3309780	1C8
ARS1-P	A1J2-54	3309780	1C7
ARS2-N	A1J2-26	3309780	1C7
ARS2-N	A1J1-26*	3309780	1C8
ARS2-N	A1U2-06	3309780	1C6
ARS2-P	A1U2-07	3309780	1C6
ARS2-P	A1J1-56*	3309780	1C8
ARS2-P	A1J2-56	3309780	1C7
ARS3-N	A1J2-27	3309780	1C7
ARS3-N	A1J1-27*	3309780	1C8
ARS3-N	A1U2-02	3309780	1C6
ARS3-P	A1U2-01	3309780	1C6
ARS3-P	A1J1-57*	3309780	1C8
ARS3-P	A1J2-57	3309780	1C7

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
ARSL-N	A1J2-22	3309780	1B7
ARSL-N	A1J1-22*	3309780	1B8
ARSL-N	A1U6-02	3309780	1B6
ARSL-P	A1U6-01	3309780	1B6
ARSL-P	A1J1-52*	3309780	1A8
ARSL-P	A1J2-52	3309780	1A7
ASCK-G	A1J3-01	3309780	3C2
ASCK-N	A1J3-02	3309780	3C2
ASCK-N	A1U20-08*	3309780	3C2
ASCK-P	A1U20-09*	3309780	3C2
ASCK-P	A1J3-14	3309780	3C2
ASCT-N	A1J3-13	3309780	3A2
ASCT-N	A1U12-04*	3309780	3A2
ASCT-P	A1U12-05*	3309780	3A2
ASCT-P	A1J3-26	3309780	3A2
ASEL-N	A1J3-22	3309780	3B2
ASEL-N	A1U12-12*	3309780	3B2
ASEL-P	A1U12-11*	3309780	3B2
ASEL-P	A1J3-09	3309780	3B2
ASKN-N	A1J3-10	3309780	3B2
ASKN-N	A1U12-13*	3309780	3B2
ASKN-P	A1U12-14*	3309780	3B2
ASKN-P	A1J3-23	3309780	3B2
-ASQ 0	A1J2-29	3309780	4A1
-ASQ 1	A1J1-29*	3309780	4A8
AWCK-G	A1J3-18	3309780	2A4
AWCK-N	A1J3-06*	3309780	2A4
AWCK-N	A1RP13-06	3309780	2A4
AWCK-P	A1RP13-19	3309780	2A4
AWCK-P	A1J3-19*	3309780	2A4
AWDT-G	A1J3-07	3309780	2B4
AWDT-N	A1J3-08*	3309780	2B4
AWDT-N	A1RP13-04	3309780	2B4
AWDT-P	A1J3-20*	3309780	2B4
AWDT-P	A1RP13-02	3309780	2B4
-B BUS 0	A5J4-16	3316180	1C7
-B BUS 0	A5U13-13*	3316180	3D6
-B BUS 0	A1J4-16	3309780	12D2
-B BUS 0	A1RP-02	3309780	2D6
-B BUS 1	A1J4-15	3309780	12D2
-B BUS 1	A1RP-08	3309780	2D6
-B BUS 1	A5J4-15	3316180	1C7
-B BUS 1	A5U13-11*	3316180	3C6
-B BUS 10	A5J4-12	3316180	1C7
-B BUS 10	A5U29-13*	3316180	3C2
-B BUS 10	A1RP1-04	3309780	2D2
-B BUS 10	A1J4-12	3309780	12C2
-B BUS 2	A1RP-03	3309780	2C6
-B BUS 2	A1J4-17	3309780	12D2
-B BUS 2	A5J4-17	3316180	1C7
-B BUS 2	A5U13-05*	3316180	3C6

TERM	ASSY/ COMPONENT/PIN	SCHM. DIAGRAM	SHEET COORD.
-B BUS 3	A5J4-18	3316180	1C7
-B BUS 3	A5U13-03*	3316180	3C6
-B BUS 3	A1RP-04	3309780	2C6
-B BUS 3	A1J4-18	3309780	12C2
-B BUS 4	A1RP-06	3309780	2B6
-B BUS 4	A5J4-20	3316180	1C7
-B BUS 4	A5U14-11*	3316180	3B6
-B BUS 4	A1J4-20	3309780	12C2
-B BUS 5	A5U14-13*	3316180	3B6
-B BUS 5	A5J4-19	3316180	1C7
-B BUS 5	A1RP-05	3309780	2B6
-B BUS 5	A1J4-19	3309780	12C2
-B BUS 6	A1J4-21	3309780	12C2
-B BUS 6	A1RP-07	3309780	2B6
-B BUS 6	A5J4-21	3316180	1C7
-B BUS 6	A5U14-05*	3316180	3B6
-B BUS 7	A5U14-03*	3316180	3A6
-B BUS 7	A5J4-22	3316180	1C7
-B BUS 7	A1RP-08	3309780	2A6
-B BUS 7	A1J4-22	3309780	12C2
-B BUS 8	A1J4-11	3309780	12C2
-B BUS 8	A5J4-11	3316180	1C7
-B BUS 8	A5U29-03*	3316180	3C2
-B BUS 9	A5U15-13*	3316180	2B4
-B BUS 9	A5J4-29	3316180	1B7
-B BUS 9	A1RP15-09	3309780	4B7
-B BUS 9	A1J4-29	3309780	12C2
-B BUS 9	A1U16-09	3309780	4B5
+B BUS 9	A5U24-12*	3316180	2B4
-B CONTROL TAG	A1U18-04	3309780	5C8
-B CONTROL TAG	A5U30-13*	3316180	3B2
-B CONTROL TAG	A5J4-42	3316180	1B7
-B CONTROL TAG	A5U23-04	3316180	5B7
-B CONTROL TAG	A1J4-42	3309780	12B2
-B PORT ENABLE	A5U29-04	3316180	3C2
-B PORT ENABLE	A5U13-04	3316180	3C6
-B PORT ENABLE	A5U30-04	3316180	3A2
-B PORT ENABLE	A5U14-04	3316180	3A6
-B PORT ENABLE	A5U8-08*	3316180	5B3
+B PORT ENABLE	A5U5-06	3316180	4A7
+B PORT ENABLE	A5U24-02*	3316180	5B2
-B PRIORITY	A5U21-06*	3316180	5C4
-B PRIORITY	A5U26-13	3316180	5A6
-B RAW SELECT	A5U7-08*	3316180	5B6
-B RAW SELECT	A5U12-13	3316180	5A7
-B RAW SELECT	A5U2-13	3316180	5B6
-B RAW SELECT	A5U27-02	3316180	5B5
-B RELEASE	A1U15-12	3309780	4B4
-B RELEASE	A1J4-24	3309780	12B2
-B RELEASE	A1U15-08	3309780	4B4
-B RELEASE	A5U23-05	3316180	5B7
-B RELEASE	A5J4-24	3316180	1C7

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-B RESERVED	A5U10-08*	3316180	5B7
-B RESERVED	A5J4-31	3316180	1B7
-B RESERVED	A1RP-08	3309780	4B7
-B RESERVED	A1J4-31	3309780	12C2
-B RESERVED	A1U16-05	3309780	4B6
+B RESERVED	A5U10-09	3316180	5B6
+B RESERVED	A1U16-06	3309780	4B6
+B RESERVED	A1U20-01	3309780	3D3
+B RESERVED	A5U4-12	3316180	5B3
+B RESERVED	A5U19-07*	3316180	5C2
+B RESERVED	A5U12-12	3316180	5A7
+B RESERVED	A5U8-09	3316180	5B2
+B RESERVED	A5U10-11	3316180	5B2
+B SEEK END	A5U25-16*	3316180	5A2
+B SEEK END	A5U33-10	3316180	4B3
-B SELECT 0	A5U17-10	3316180	5C7
-B SELECT 0	A5U16-13*	3316180	2D4
-B SELECT 1	A5U16-11*	3316180	2D4
-B SELECT 1	A5U17-12	3316180	5C7
-B SELECT 2	A5U17-13	3316180	5C7
-B SELECT 2	A5U16-05*	3316180	2C4
-B SELECT 3	A5U17-15	3316180	5C7
-B SELECT 3	A5U16-03*	3316180	2C4
-B SELECT ENABLE	A5U24-11	3316180	5B7
-B SELECT ENABLE	A5U8-05	3316180	5B7
-B SELECT ENABLE	A5U23-11*	3316180	2B4
-B SELECTED	A1R15-05	3309780	4C7
-B SELECTED	A1U15-02	3309780	4C3
-B SELECTED	A1J4-27	3309780	12C2
-B SELECTED	A5U12-05	3316180	5B4
-B SELECTED	A5U11-06*	3316180	5B4
-B SELECTED	A5J4-27	3316180	1B7
+B SELECTED	A5U31-03	3316180	4C3
+B SELECTED	A5U18-13	3316180	5A4
+B SELECTED	A5U11-05*	3316180	5B5
+B SELECTED	A5U32-15	3316180	4B3
+B SELECTED	A5U22-03	3316180	5B5
BB10-N	A5RN10-07	3316180	3C4
BB10-N	A5J1-30*, A5J2-30	3316180	3C4
BB10-P	A5RN10-06	3316180	3C4
BB10-P	A5J1-60*, A5J2-60	3316180	3C4
BBS0-N	A5RN4-01	3316180	3D7
BBS0-N	A5J1-04*, A5J2-04	3316180	3D8
BBS0-P	A5J1-34*, A5J2-34	3316180	3D8
BBS0-P	A5RN4-03	3316180	3D7
BBS1-N	A5RN4-05	3316180	3D7
BBS1-N	A5J1-05*, A5J2-05	3316180	3D8
BBS1-P	A5J1-35*, A5J2-35	3316180	3C8
BBS1-P	A5RN4-07	3316180	3D7
BBS2-N	A5RN5-05	3316180	3C7
BBS2-N	A5J1-06*, A5J2-06	3316180	3C8

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
BBS2-P	A5J1-36*, A5J2-36	3316180	3C8
BBS2-P	A5RN5-07	3316180	3C7
BBS3-N	A5RN5-01	3316180	3C7
BBS3-N	A5J1-07*, A5J2-07	3316180	3C8
BBS3-P	A5J1-37*, A5J2-37	3316180	3C8
BBS3-P	A5RN5-03	3316180	3C7
BBS4-N	A5RN6-05	3316180	3B7
BBS4-N	A5J1-08*, A5J2-08	3316180	3B7
BBS4-P	A5J1-38*, A5J2-38	3316180	3B7
BBS4-P	A5RN6-07	3316180	3B7
BBS5-N	A5RN6-01	3316180	3B7
BBS5-N	A5J1-09*, A5J2-09	3316180	3B7
BBS5-P	A5J1-39*, A5J2-39	3316180	3B7
BBS5-P	A5RN6-03	3316180	3B7
BBS6-N	A5RN7-05	3316180	3A7
BBS6-N	A5J1-10*, A5J2-10	3316180	3B7
BBS6-P	A5J1-40*, A5J2-40	3316180	3B7
BBS6-P	A5RN7-07	3316180	3A7
BBS7-N	A5RN7-01	3316180	3A7
BBS7-N	A5J1-11*, A5J2-11	3316180	3A7
BBS7-P	A5J1-41*, A5J2-41	3316180	3A7
BBS7-P	A5RN7-03	3316180	3A7
BBS8-N	A5RN11-07	3316180	3D4
BBS8-N	A5J1-12*, A5J2-12	3316180	3D4
BBS8-P	A5RN11-05	3316180	3D4
BBS8-P	A5J1-42*, A5J2-42	3316180	3C4
BBS9-N	A5RN8-03	3316180	2B6
BBS9-N	A5J1-13*, A5J2-13	3316180	2B7
BBS9-P	A5J1-43*, A5J2-43	3316180	2B7
BBS9-P	A5RN8-01	3316180	2B6
BFT1-N	A5RN10-03	3316180	3C4
BFT1-N	A5J1-01*, A5J2-01	3316180	3C4
BFT1-P	A5J1-31*, A5J2-31	3316180	3C4
BFT1-P	A5RN10-01	3316180	3C4
BFT2-N	A5RN11-03	3316180	3C4
BFT2-N	A5J1-02*, A5J2-02	3316180	3C4
BFT2-P	A5J1-32*, A5J2-32	3316180	3C4
BFT2-P	A5RN11-01	3316180	3C4
BFT3-N	A5RN12-01	3316180	3B4
BFT3-N	A5J1-03*, A5J2-03	3316180	3B4
BFT3-P	A5J1-33*, A5J2-33	3316180	3B4
BFT3-P	A5RN12-03	3316180	3B4
-BHL 0	A5J2-59	3316180	4A5
-BHL 0	A1CR4	3309780	4A7
-BHL 1	A1RP15-04	3309780	4B7
-BHLO	A5J4-02	3316180	1D7
-BHLO	A1J4-02	3309780	12B2
-BHL1	A1J4-01	3309780	12C2
-BHL1	A5J4-01	3316180	1D7
BHL1	A5J1-59*, A5J2-59	3316180	2A7
BIDX-N	A5J3-12	3316180	4B1
BIDX-N	A5U33-04*	3316180	4B2

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
BIDX-P	A5J3-24	3316180	4B1
BIDX-P	A5U33-05*	3316180	4B2
+BRAKE COIL	A6J2-01	3309790	3C3
+BRAKE COIL	A6Q15-C*	3309790	3C6
-BRAKE RETN	A6J2-02	3309790	3C3
BRCK-N	A5J3-17	3316180	4C1
BRCK-N	A5U32-09*	3316180	4C2
BRCK-P	A5U32-08*	3316180	4C2
BRCK-P	A5J3-05	3316180	4C1
BRDT-N	A5U32-12*	3316180	4C2
BRDT-N	A5J3-16	3316180	4C1
BRDT-P	A5J3-03	3316180	4C1
BRDT-P	A5U32-13*	3316180	4C2
BRDV-N	A5RN8-05	3316180	2C6
BRDV-N	A5J1-14*, A5J2-14	3316180	2C7
BRDV-P	A5J1-44*, A5J2-44	3316180	2C7
BRDV-P	A5RN8-07	3316180	2C6
BRSO-N	A5RN2-05	3316180	2D6
BRSO-N	A5J1-23*, A5J2-23	3316180	2D7
BRSO-P	A5J1-53*, A5J2-53	3316180	2D7
BRSO-P	A5RN2-07	3316180	2D6
BRS1-N	A5RN2-01	3316180	2D6
BRS1-N	A5J1-24*, A5J2-24	3316180	2D7
BRS1-P	A5J1-54*, A5J2-54	3316180	2D7
BRS1-P	A5RN2-03	3316180	2D6
BRS2-N	A5RN3-05	3316180	2C6
BRS2-N	A5J1-26*, A5J2-26	3316180	2C7
BRS2-P	A5J1-56*, A5J2-56	3316180	2C7
BRS2-P	A5RN3-07	3316180	2C6
BRS3-N	A5RN3-01	3316180	2C6
BRS3-N	A5J1-27*, A5J2-27	3316180	2C7
BRS3-P	A5J1-57*, A5J2-57	3316180	2C7
BRS3-P	A5RN3-03	3316180	2C6
BBSL-N	A5RN9-03	3316180	2B6
BBSL-N	A5J1-22*, A5J2-22	3316180	2B7
BBSL-P	A5RN9-01	3316180	2B6
BBSL-P	A5J1-52*, A5J2-52	3316180	2B7
BBSCK-G	A5J3-01	3316180	4C2
BBSCK-N	A5U31-09*	3316180	4C2
BBSCK-N	A5J3-14	3316180	4C1
BBSCK-P	A5U31-08*	3316180	4C2
BBSCK-P	A5J3-02	3316180	4C1
BBSCT-N	A5U33-03*	3316180	4B3
BBSCT-N	A5J3-13	3316180	4B2
BBSCT-P	A5U33-02*	3316180	4A3
BBSCT-P	A5J3-16	3316180	4A2
BSEL-N	A5J3-22	3316180	4B1
BSEL-N	A5U33-13*	3316180	4B2
BSEL-P	A5U33-14*	3316180	4B2
BSEL-P	A5J3-09	3316180	4B1
BBSKN-N	A5J3-10	3316180	4B1
BBSKN-N	A5U33-12*	3316180	4B2

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
BSKN-P	A5U33-11*	3316180	4B2
BSKN-P	A5J3-23	3316180	4B1
-BSQ 1	U1J2-29	3309780	4A1
-BSQ0	A1K1-07	3309780	4A2
-BSQ0	A1J4-04	3309780	12B2
-BSQ0	A5J4-04	3316180	1D7
-BSQ1	A5J1-29*, A5J2-29	3316180	2A7
-BSQ1	A5J4-03	3316180	1D7
-BSQ1	A1J4-03	3309780	12C2
-BUS 0	A1U14-13	3309780	5C7
-BUS 0	A1RP-02*	3309780	2D5
+BUS 0	A1U37-04	3309780	5C6
+BUS 0	A1U55-13	3309780	5D6
+BUS 0	A1U14-12*	3309780	5C7
+BUS 0	A1U45-03	3309780	7D7
+BUS 1	A1U55-11	3309780	5D6
+BUS 1	A1U37-09	3309780	5D6
+BUS 1	A1U14-04*	3309780	5C7
+BUS 1	A1U45-04	3309780	7D7
-BUS 1	A1U14-03	3309780	5C7
-BUS 1	A1RP-08*	3309780	2D5
-BUS 10	A1RP1-04*	3309780	2D2
+BUS 10	A1U14-05	3309780	7C7
+BUS 2	A1U36-09	3309780	5D6
+BUS 2	A1U14-02*	3309780	5B7
+BUS 2	A1U45-07	3309780	7D7
+BUS 2	A1U55-06	3309780	5D6
-BUS 2	A1U14-01	3309780	5B7
-BUS 2	A1RP-03*	3309780	2C5
-BUS 3	A1U13-01	3309780	5B7
-BUS 3	A1RP-04*	3309780	2C5
+BUS 3	A1U36-13	3309780	5B6
+BUS 3	A1U13-02*	3309780	5B7
+BUS 3	A1U45-08	3309780	7D7
+BUS 3	A1U55-04	3309780	5D6
+BUS 4	A1U13-06*	3309780	5B7
+BUS 4	A1U45-13	3309780	7D7
+BUS 4	A1U33-04	3309780	5B6
-BUS 4	A1RP-06*	3309780	2B4
-BUS 4	A1U13-05	3309780	5B7
-BUS 5	A1U14-09	3309780	5B7
-BUS 5	A1RP-05*	3309780	2B4
+BUS 5	A1U14-08*	3309780	5B7
+BUS 5	A1U45-14	3309780	7D7
+BUS 5	A1U33-12	3309780	5B6
+BUS 6	A1U45-17	3309780	7C7
BUS 6	A1U13-10*	3309780	5C5
-BUS 6	A1U13-11	3309780	5C5
-BUS 6	A1RP-07*	3309780	2B6
-BUS 7	A1RP-08*	3309780	2A6
-BUS 7	A1U13-09	3309780	5B7
+BUS 7	A1U13-08*	3309780	5B7

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
+BUS 7	A1U45-18	3309780	7C7
+BUS 7	A1U33-09	3309780	5B6
+BUS 8	A1U44-03	3309780	7C7
+BUS 8	A1U14-10*	3309780	5A7
+BUS 8	A1U33-01	3309780	5A6
-BUS 8	A1U14-11	3309780	5A7
-BUS 8	A1RP1-05	3309780	2D2
-BUS 9	A1U16-11	3309780	4B5
+BUS 9	A1U44-04	3309780	7C7
+BUS 9	A1U15-11*	3309780	4B4
BWCK-G	A5RN14-01	3316180	3A4
BWCK-G	A5J3-18*	3316180	3A4
BWCK-N	A5J3-06*	3316180	3A4
BWCK-N	A5RN14-05	3316180	3A4
BWCK-P	A5RN14-07	3316180	3A4
BWCK-P	A5J3-19*	3316180	3A4
BWDT-G	A5J3-07*	3316180	3A4
BWDT-G	A5RN14-01	3316180	3A4
BWDT-N	A5RN14-03	3316180	3A4
BWDT-N	A5J3-08*	3316180	3A4
BWDT-P	A5J3-20*	3316180	3A4
BWDT-P	A5RN14-02	3316180	3A4
+CAR 1	A1J5-19	3309780	12C7
+CAR 1	A3J3-17	3309770	6B8
+CAR 1	A3U34-02	3309770	6A8
+CAR 1	A1U42-02*	3309780	7C4
+CAR 2	A3J3-19	3309770	6B8
+CAR 2	A3U34-03	3309770	6A8
+CAR 2	A1U42-05*	3309780	7C4
+CAR 2	A1J5-17	3309780	12C7
-CEMH 0 (CHIP EN 0)	A2J2-12	3309760	2A1
-CEMH 0 (CHIP EN 0)	A2U59-04*	3309760	2A4
-CEMH 1 (CHIP ENABLE 1)	A2J2-14	3309760	2A1
-CEMH 1 (CHIP ENABLE 1)	A2U59-03*	3309760	2A4
-CEMH 2 (CHIP ENABLE 2)	A2U59-02*	3309760	2A4
-CEMH 2 (CHIP ENABLE 2)	A2J2-16	3309760	2A1
-CEMH 3 (CHIP ENABLE 3)	A2U59-01*	3309760	2A4
-CEMH 3 (CHIP ENABLE 3)	A2J2-18	3309760	2A1
-CHIP EN 0 (CEMH 0)	A7J1-12	3309800	1C3
-CHIP ENABLE 1 (CEMH 1)	A7J1-14	3309800	1C3
-CHIP ENABLE 2 (CEMH 2)	A7J1-16	3309800	1C3
-CHIP ENABLE 3 (CEMH 3)	A7J1-18	3309800	1C3
-COLUMN X1	A1J8-02	3309780	12C4
-COLUMN X1	A1U120-11	3309780	10A6
-COLUMN X1	A4J1-02	3310060	1A8
-COLUMN X1	A4KEYBD-01*	3310060	1A7
-COLUMN X2	A4J1-01	3310060	1A7
-COLUMN X2	A4KEYBD-02*	3310060	1A7
-COLUMN X2	A1J8-01	3309780	12C4
-COLUMN X2	A1U120-10	3309780	10A6

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-COLUMN X3	A1J8-04	3309780	12C4
-COLUMN X3	A1U120-08	3309780	10A6
-COLUMN X3	A4J1-04	3310060	1A8
-COLUMN X3	A4KEYBD-03*	3310060	1A6
-COLUMN X4	A4KEYBD-04*	3310060	1A6
-COLUMN X4	A4J1-03	3310060	1A7
-COLUMN X4	A1J8-03	3309780	12C4
-COLUMN X4	A1U120-07	3309780	10A6
-CONTROLLER RESET	A1U33-06	3309780	5B6
-CONTROLLER RESET	A1U77-05	3309780	10C4
CURRENT SENSE	A3J2-02	3309770	7A3
CURRENT SENSE	A3R138	3309770	7A6
CURRENT SENSE	A3R92	3309770	5A6
CYL PULSE	A3J3-12	3309770	5D1
CYL PULSE	A3U34-14	3309770	5C5
-CYL PULSE	A1U32-05	3309780	8A3
-CYL PULSE	A1U32-12	3309780	8B3
-CYL TRANS	A1J5-12	3309780	12C7
CYL TRANS	A3U43-08*	3309770	5C6
+CYLINDER TAG	A1U44-11	3309780	7C7
+CYLINDER TAG	A1U45-11	3309780	7C7
-CYLINDER TAG	A1U3-03*	3309780	2C2
-CYLINDER TAG	A1RP1-06	3309780	2C2
-CYLINDER TAG	A5U29-11*	3316180	3C2
-CYLINDER TAG	A5J4-13	3316180	1C7
-CYLINDER TAG	A1J4-13	3309780	12C2
-CYLINDER TAG	A1U39-11	3309780	5A4
-D BUS 0	A1RP-02	3309780	2D6
-D BUS 0	A1U22-03*	3309780	11A5
-D BUS 0	A1U24-11*	3309780	11D2
-D BUS 1	A1U24-03*	3309780	11D2
-D BUS 1	A1RP-08	3309780	2D6
-D BUS 1	A1U23-12*	3309780	11A5
-D BUS 2	A1U24-06*	3309780	11D2
-D BUS 2	A1RP-03	3309780	2C6
-D BUS 3	A1U24-08*	3309780	11D2
-D BUS 3	A1RP-04	3309780	2C6
-D BUS 5	A1RP-05	3309780	2B6
-D BUS 5	A1U23-08*	3309780	11B2
-D CONTROL TAG	A1U18-05	3309780	5C8
-D CONTROL TAG	A1U100-06*	3309780	11A6
+D1SA	A4DS1-10	3310060	1D3
+D1SA	A4J1-25	3310060	1D4
+D1SA	A1J8-25	3309780	12C4
+D1SA	A1U123-13*	3309780	10A2
+D1SB	A1J8-26	3309780	12C4
+D1SB	A1U123-12*	3309780	10A2
+D1SB	A4SD-09	3310060	1D3
+D1SB	A4J1-26	3310060	1D4

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
+D1SC	A1J8-27	3309780	12C4
+D1SC	A1U123-11*	3309780	10A2
+D1SC	A4J1-27	3310060	1D4
+D1SC	A4DS1-08	3310060	1D3
+D1SD	A4DS1-05	3310060	1D3
+D1SD	A4J1-28	3310060	1D4
+D1SD	A1J8-28	3309780	12C4
+D1SD	A1U123-10*	3309780	10A2
+D1SE	A1J8-29	3309780	12C4
+D1SE	A1U123-09*	3309780	10A2
+D1SE	A4DS1-04	3310060	1D3
+D1SE	A4J1-29	3310060	1D4
+D1SF	A1U123-15*	3309780	10A2
+D1SF	A4DS1-02	3310060	1D3
+D1SF	A4J1-23	3310060	1D4
+D1SF	A1J8-23	3309780	12C4
+D1SG	A4DS1-03	3310060	1D3
+D1SG	A4J1-24	3310060	1D4
+D1SG	A1J8-24	3309780	12C4
+D1SG	A1U123-14*	3309780	10A2
+D2SA	A1J8-20	3309780	12C4
+D2SA	A1U122-13*	3309780	10A3
+D2SA	A4J1-20	3310060	1D5
+D2SA	A4DS2-10	3310060	1D5
+D2SB	A1U122-12*	3309780	10A3
+D2SB	A4J1-16	3310060	1D5
+D2SB	A4DS2-09	3310060	1D5
+D2SB	A1J8-16	3309780	12C4
+D2SC	A1J8-17	3309780	12C4
+D2SC	A1U122-11*	3309780	10A3
+D2SC	A4J1-17	3310060	1D5
+D2SC	A4DS2-06	3310060	1D5
+D2SD	A4J1-18	3310060	1D5
+D2SD	A1J8-18	3309780	12C4
+D2SD	A1U122-10*	3309780	10A3
+D2SD	A4DS2-05	3310060	1D5
+D2SE	A1U122-09*	3309780	10A3
+D2SE	A4J1-19	3310060	1D5
+D2SE	A4DS2-04	3310060	1D5
+D2SE	A1J8-19	3309780	12C4
+D2SF	A4DS2-02	3310060	1D5
+D2SF	A4J1-22	3310060	1D5
+D2SF	A1J8-22	3309780	12C4
+D2SF	A1U122-15*	3309780	10A3
+D2SG	A1J8-21	3309780	12C4
+D2SG	A1U122-14*	3309780	10A3
+D2SG	A4DS2-03	3310060	1D5
+D2SG	A4J1-21	3310060	1D5
+D3SA	A1U124-13*	3309780	10A4
+D3SA	A4J1-32	3310060	1D6
+D3SA	A4DS3-10	3310060	1D6
+D3SA	A1J8-32	3309780	12C4

TERM	ASSY/ COMPONENT/PIN	SCHED. DIAGRAM	SHEET COORD.
+D3SB	A4J1-33	3310060	1D6
+D3SB	A4DS3-09	3310060	1D6
+D3SB	A1J8-33	3309780	12B4
+D3SB	A1U124-12*	3309780	10A4
+D3SC	A1J8-34	3309780	12B4
+D3SC	A1U124-11*	3309780	10A4
+D3SC	A4J1-34	3310060	1D6
+D3SC	A4DS3-08	3310060	1D6
+D3SD	A1U124-10*	3309780	10A4
+D3SD	A4J1-35	3310060	1D6
+D3SD	A4DS3-05	3310060	1D6
+D3SD	A1J8-35	3309780	12B4
+D3SE	A4J1-36	3310060	1D6
+D3SE	A4DS3-04	3310060	1D6
+D3SE	A1J8-36	3309780	12B4
+D3SE	A1U124-09*	3309780	10A4
+D3SF	A1U124-15*	3309780	10A4
+D3SF	A4J1-36	3310060	1D6
+D3SF	A4DS3-02	3310060	1D6
+D3SG	A1U124-14*	3309780	10A4
+D3SG	A1J8-31	3309780	12B4
+D3SG	A4J1-31	3310060	1D6
+D3SG	A4DS3-03	3310060	1D6
+D4SA	A4DS4-10	3310060	1D7
+D4SA	A4J1-13	3310060	1D7
+D4SA	A1U121-13*	3309780	10A5
+D4SA	A1J8-13	3309780	12B4
+D4SB	A1J8-12	3309780	12B4
+D4SB	A1U121-12*	3309780	10A5
+D4SB	A4DS4-09	3310060	1D7
+D4SB	A4J1-12	3310060	1D7
+D4SC	A4DS4-08	3310060	1D7
+D4SC	A4J1-11	3310060	1D7
+D4SC	A1J8-11	3309780	12B4
+D4SC	A1U121-11*	3309780	10A5
+D4SD	A1J8-09	3309780	12B4
+D4SD	A1U121-10*	3309780	10A5
+D4SD	A4J1-09	3310060	1D7
+D4SD	A4DS4-05	3310060	1D7
+D4SE	A1J8-10	3309780	12B4
+D4SE	A1U121-09*	3309780	10A5
+D4SE	A4J1-10	3310060	1D7
+D4SE	A4DS4-04	3310060	1D7
+D4SF	A1J8-15	3309780	12B4
+D4SF	A1U121-15*	3309780	10A5
+D4SF	A4DS4-02	3310060	1D7
+D4SF	A4J1-15	3310060	1D7
+D4SG	A4J1-14	3310060	1D7
+D4SG	A4DS4-03	3310060	1D7
+D4SG	A1J8-14	3309780	12B4
+D4SG	A1U121-14*	3309780	10A5

TERM	ASSY/ COMPONENT/PIN	SCHM. DIAGRAM	SHEET COORD.
+DATA AVAILABLE	A1U120-12*	3309780	10B6
+DATA AVAILABLE	A1U87-17	3309780	7B7
+DATA HOLD	A2U47-03*	3309760	5B7
+DATA HOLD	A2U5-15	3309760	3A3
DATA X (DX)	A7J1-03	3309800	1D3
DATA Y (DY)	A7J1-02	3309800	1D3
+DHAR 1	A1U46-02*	3309780	11D7
+DHAR 2	A1U46-05*	3309780	11D7
+DHAR 4	A1U46-06*	3309780	11D7
+DHAR 8	A1U46-09*	3309780	11D7
+DHAR1	A1U24-12	3309780	11D2
+DHAR2	A1U24-01	3309780	11D2
+DHAR4	A1U24-04	3309780	11D2
+DHAR8	A1U24-09	3309780	11D2
-DIAGNOSTIC (DIAGNOSTICS SWITCH)	A4J1-37	3310060	1B7
-DIAGNOSTIC (DIAGNOSTICS SWITCH)	A4S1*	3310060	1B7
-DIAGNOSTICS	A1U59-09	3309780	11B5
-DIAGNOSTICS	A1U18-01	3309780	4C3
-DIAGNOSTICS	A1J4-30	3309780	12B2
-DIAGNOSTICS	A1U17-08*	3309780	4C6
-DIAGNOSTICS	A1U17-13	3309780	4B6
-DIAGNOSTICS	A5U18-04	3316180	5D2
-DIAGNOSTICS	A5J4-30	3316180	1C7
-DIAGNOSTICS	A5U8-10	3316180	5B3
-DIAGNOSTICS SWITCH (DIAGNOSTIC)	A1R15-07	3309780	4C8
-DIAGNOSTICS SWITCH (DIAGNOSTIC)	A1J8-37	3309780	12C4
-DIAGNOSTICS SWITCH (DIAGNOSTIC)	A1U17-10	3309780	4C8
-DIAGNOSTICS TEST	A1U43-02*	3309780	7B3
-DIAGNOSTICS TEST	A1U17-09	3309780	4C7
-DIAGONSTICS	A1U87-18	3309780	7B7
-DIFF 1 (-1)	A1J5-34	3309780	12C7
-DIFF 1 (-1)	A1U19-03*	3309780	7C2
DIFF 1024	A1J5-04	3309780	12C7
-DIFF 1024 (-1024)	A1U30-06*	3309780	7D2
-DIFF 128 (-128)	A1U31-07*	3309780	7C2
DIFF 128 (-128)	A1J5-27	3309780	12C7
-DIFF 16 (-16)	A1U31-03*	3309780	7C2
-DIFF 16 (-16)	A1J5-32	3309780	12C7
-DIFF 2 (-2)	A1U19-02*	3309780	7B2
-DIFF 2 (-2)	A1J5-33	3309780	12C7
-DIFF 256	A1J5-06	3309780	12C7
-DIFF 256 (-256)	A1U30-03*	3309780	7D2
-DIFF 32 (-32)	A1U31-02*	3309780	7C2
-DIFF 32 (-32)	A1J5-30	3309780	12C7
-DIFF 4 (-4)	A1J5-31	3309780	12C7
-DIFF 4 (-4)	A1U19-06*	3309780	7B2
-DIFF 512 (-512)	A1J5-08	3309780	12C7
-DIFF 512 (-512)	A1U30-02*	3309780	7D2
-DIFF 64 (-64)	A1U3-06*	3309780	7C2
-DIFF 64 (-64)	A1J5-28	3309780	12C7
-DIFF 8 (-8)	A1U19-07*	3309780	7B2
-DIFF 8 (-8)	A1J5-29	3309780	12C7

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-DIFF <>0	A1U69-08*	3309780	7D2
+DIFF <>0	A1U68-08*	3309780	7C2
-DIFF #0	A1J5-20	3309780	12C7
-DIFF #0	A3U25-05	3309770	6A7
-DIFF #0	A3U3-01	3309770	6C3
-DIFF #0	A3J3-20	3309770	6A8
-DIFF #0	A3U5-01	3309770	6C4
-DIFF CLOCK	A1U25-10*	3309780	8B3
-DIFF CLOCK	A1U9-05	3309780	7A5
-DIFF CLOCK	A1U9-11	3309780	7A4
+DIFF#0	A1U86-07	3309780	7D6
-DISABLE A	A1U17-11*	3309780	4B6
-DISABLE A	A1U21-10	3309780	3A10
-DISABLE A	A1U16-13	3309780	1A7
-DISABLE A	A1U12-06	3309780	3A3
-DISABLE A	A1U20-10	3309780	3D3
-DISABLE B	A5U24-09	3316180	2A5
-DISABLE B	A5U31-10, A5U32-10	3316180	4C3
-DISABLE B	A5U33-06	3316180	4A3
-DISABLE B	A5U18-06*	3316180	5D2
DX (DATA X)	A2J2-03	3309760	4C8
DX (DATA X)	A2Q10B	3309760	4C7
DX (DATA X)	A2Q13C	3309760	4C7
DY (DATA Y)	A2Q12C	3309760	4C8
DY (DATA Y)	A2J2-02	3309760	4C8
+EN SEQ TNU	A1U23-03	3309780	4A3
+EN SEQ TNU	A1U42-15*	3309780	7C4
-ERROR 1	A1U85-03	3309780	7C7
-ERROR 1	A1U84-09*	3309780	10D6
-ERROR 2	A1U85-04	3309780	7C7
-ERROR 2	A1U84-07*	3309780	10D6
-ERROR 4	A1U84-06*	3309780	10D6
-ERROR 4	A1U85-07	3309780	7B7
ERROR AMP	A3U6-07*	3309770	6B2
ERROR AMPLIFIER	A3R137	3309770	7C7
ERROR AMPLIFIER	A3U33-06	3309770	7C7
-FAULT LED (-UNSAFE LED)	A4J1-43	3310060	1B7
-FAULT LED (-UNSAFE LED)	A4DS7-C	3310060	1B7
-FAULT RESET SW	A4S2*	3310060	1A7
-FAULT RESET SW	A1J8-42	3309780	12C4
-FAULT RESET SW	A1U77-04	3309780	10C4
-FAULT RESET SW	A4J1-42	3310060	1B7
+FEEDBACK PULSE TTL	A348-11	3309770	2B8
+FEEDBACK PULSE TTL	A3U82-09*	3309770	3B4
+FILE READY	A1J4-39	3309780	12C2
+FILE READY	A5J4-39	3316180	1B7
+FILE READY	A1U17-03*	3309780	10D1
+FILE READY	A1U8-10	3309780	3C8
+FILE READY	A5U6-15	3316180	4B7
-FINE TRACK	A1U83-13	3309780	10C6
-FINE TRACK	A1U75-04	3309780	10C7
-FINE TRACK	A1U86-08	3309780	7D6

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-FINE TRACK	A3J3-15	3309770	6B1
-FINE TRACK	A3U25-04*	3309770	6B3
-FINE TRACK	A1J5-15	3309780	12C7
-GATE 1	A3U81-06*	3309770	3B3
-GATE 1	A3R170	3309770	4D8
-GATE 2	A3U81-12*	3309770	3C3
-GATE 2	A3R219	3309770	4D8
-GATE 3	A3U81-08*	3309770	3C3
-GATE 3	A3R232	3309770	4B8
-GATE 4	A3R227	3309770	4B8
-GATE 4	A3U81-10*	3309770	3C3
-GATED MULT HD (-MULTI CHIP SEL)	A2U50-03*	3309760	1B3
-GATED MULT HD (-MULTI CHIP SEL)	A2J1-24	3309760	1B3
-GATED R/W UNSAFE (-R/W UNSAFE)	A2U50-06*	3309760	1B3
-GATED R/W UNSAFE (-R/W UNSAFE)	A2J1-16	3309760	1B3
-GATED WRITE	A2U39-06*	3309760	1B3
-GATED WRITE	A2U6-05	3309760	1B4
-GATED WRITE	A2U6-11	3309760	2D7
-GATED WRITE	A2U65-10	3309760	4B7
-GATED WRITE	A2U65-09	3309760	4B7
-GATED WS	A2U66-02	3309760	4B5
-GATED WS	A2U6-04*	3309760	1B3
+GATED WS	A2U6-02*	3309760	1B3
+GATED WS	A2U66-04	3309760	4B4
+GB ERROR	A1U87-14	3309780	7B7
+GB ERROR	A1U76-09*	3309780	8C3
-H VEL	A3U54-07	3309770	4C8
-H VEL	A3U66-01*,02*	3309770	5B2
-H VEL	A3U65-09,01	3309770	5B8
-HAR 1	A2U64-10	3309760	4A7
-HAR 1	A257-11	3309760	4A4
-HAR 1	A1U63-04*	3309780	5C5
-HAR 1	A1J6-33	3309780	12C5
-HAR 1	A2J1-33	3309760	4A8
-HAR 2	A2U57-10	3309760	4B4
-HAR 2	A2J1-34	3309760	4A8
-HAR 2	A1J6-34	3309780	12C5
-HAR 2	A1U63-07*	3309780	5C5
-HAR 4	A1U63-09*	3309780	5C5
-HAR 4	A2J1-31	3309760	2A8
-HAR 4	A1J6-31	3309780	12C5
HAR 4 (-HAR 4)	A2U59-15	3309760	2A4
-HAR 8	A1J6-32	3309780	12C5
-HAR 8	A2J1-32	3309760	2A8
-HAR 8	A1U63-12*	3309780	5C5
HAR 8 (-HAR 8)	A2U59-14	3309760	2A4
-HD TAG (-HEAD TAG)	A2U50-12	3309760	1B7
-HD TAG (-HEAD TAG)	A2J1-14	3309760	1B8
-HD TAG (-HEAD TAG)	A1J6-14	3309780	12C5
-HD TAG (-HEAD TAG)	A2U40-03	3309760	1B7
-HEAD SELECT 1 (-HS1)	A7J1-10	3309800	1C3
-HEAD SELECT 2 (-HS2)	A7J1-05	3309800	1D3

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-HEAD TAG (-HD TAG)	A1U3-05*	3309780	2C2
-HEAD TAG (-HD TAG)	A1RP1-07	3309780	2C2
-HEAD TAG (-HD TAG)	A1U13-03	3309780	5D7
-HEAD TAG (-HD TAG)	A1U22-06*	3309780	11C2
-HEAD TAG (-HD TAG)	A5J4-14	3316180	1C7
-HEAD TAG (-HD TAG)	A5U29-05*	3316180	3C2
-HEAD TAG (-HD TAG)	A1J4-14	3309780	12C2
+HOLD	A2U34-08	3309760	5B2
+HOLD	A2U46-02*	3309760	5B2
+HOLD	A2U29-13	3309760	3B7
-HS1 (-HEAD SELECT 1)	A2J2-10	3309760	4A1
-HS1 (-HEAD SELECT 1)	A2U67-13*	3309760	4A2
-HS2 (-HEAD SELECT 2)	A2J2-05	3309760	4B1
-HS2 (-HEAD SELECT 2)	A2U61-13*	3309760	4B2
I/O BUS	A1U45-15*	3309780	7D7
I/O BUS	A1U87-05*	3309780	7B7
I/O BUS	A1U86-05*	3309780	7D5
I/O BUS	A1U121-07,01,02,06	3309780	10A5
I/O BUS	A1U46-13,14,17,18	3309780	11D7
I/O BUS	A1U46-03,04,07,08	3309780	11D7
I/O BUS	A1U86-19*	3309780	7D5
I/O BUS	A1U44-15*	3309780	7C7
I/O BUS	A1U41-03*	3309780	7D4
I/O BUS	A1U50-03,04,07,08	3309780	11D5
I/O BUS	A1U56-03,04,07,08	3309780	11D6
I/O BUS	A1U44-09*	3309780	7C7
I/O BUS	A1U87-09*	3309780	7B7
I/O BUS	A1U87-02*	3309780	7B7
I/O BUS	A1U122-07,01,02,06	3309780	10A3
I/O BUS	A1U124-07,01,02,06	3309780	10A4
I/O BUS	A1U44-12*	3309780	7C7
I/O BUS	A1U85-02*	3309780	7C7
I/O BUS	A1U44-06*	3309780	7C7
I/O BUS	A1U86-12*	3309780	7D5
I/O BUS	A1U86-15*	3309780	7D5
I/O BUS	A1U44-05*	3309780	7C7
I/O BUS	A1U123-07,01,02,06	3309780	10A2
I/O BUS	A1U43-18*	3309780	7C4
I/O BUS	A1U119-12*	3309780	7C5
I/O BUS	A1U85-05*	3309780	7C7
I/O BUS	A1U113-03,04,07,08	3309780	11B6
I/O BUS	A1U85-12*	3309780	7C7
I/O BUS	A1U65-11* THRU 18*	3309780	6B3
I/O BUS	A1U64-15*	3309780	7C5
I/O BUS	A1U85-09*	3309780	7C7
I/O BUS	A1U64-16*	3309780	7C5
I/O BUS	A1U44-02*	3309780	7C7
I/O BUS	A1U85-16*	3309780	7C7
I/O BUS	A1U64-02*	3309780	7C5
I/O BUS	A1U119-05*	3309780	7C5
I/O BUS	A1U119-15*	3309780	7C5
I/O BUS	A1U85-15*	3309780	7C7

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
I/O BUS	A1U119-19*	3309780	7C5
I/O BUS	A1U86-02*	3309780	7D5
I/O BUS	A1U119-16*	3309780	7C5
I/O BUS	A1U113-13, 14, 17, 18	3309780	11B6
I/O BUS	A1U43-17*	3309780	7C4
I/O BUS	A1U119-02*	3309780	7C5
I/O BUS	A1U85-19*	3309780	7C7
I/O BUS	A1U43-08*	3309780	7C4
I/O BUS	A1U86-06*	3309780	7D5
I/O BUS	A1U30-09*	3309780	7D3
I/O BUS	A1U64-06*	3309780	7C5
I/O BUS	A1U119-09*	3309780	7C5
I/O BUS	A1U43-13*	3309780	7C4
I/O BUS	A1U86-09*	3309780	7D5
I/O BUS	A1U119-06*	3309780	7C5
I/O BUS	A1U43-04*	3309780	7C4
I/O BUS	A1U43-07*	3309780	7C4
I/O BUS	A1U45-19*	3309780	7D7
I/O BUS	A1U64-09*	3309780	7C5
I/O BUS	A1U30-10*	3309780	7D3
I/O BUS	A1U31-15*	3309780	7C3
I/O BUS	A1U43-03*	3309780	7C4
I/O BUS	A1U64-05*	3309780	7C5
I/O BUS	A1U85-06*	3309780	7C7
I/O BUS	A1U30-15*	3309780	7D3
I/O BUS	A1U31-10*	3309780	7C3
I/O BUS	A1U31-01*	3309780	7C3
I/O BUS	A1U31-09*	3309780	7C3
I/O BUS	A1U42-18*	3309780	7C4
I/O BUS	A1U45-16*	3309780	7D7
I/O BUS	A1U44-16*	3309780	7C7
I/O BUS	A1U41-17*	3309780	7D4
I/O BUS	A1U45-12*	3309780	7D7
I/O BUS	A1U86-16*	3309780	7D5
I/O BUS	A1U87-19*	3309780	7B7
I/O BUS	A1U42-13*	3309780	7C4
I/O BUS	A1U30-01*	3309780	7D3
I/O BUS	A1U42-14*	3309780	7C4
I/O BUS	A1U42-17*	3309780	7C4
I/O BUS	A1U42-07*	3309780	7C4
I/O BUS	A1U97-02, 05, 06, 09	3309780	11C1
I/O BUS	A1U41-18*	3309780	7D4
I/O BUS	A1U45-06*	3309780	7D7
I/O BUS	A1U42-08*	3309780	7C4
I/O BUS	A1U64-19*	3309780	7C5
I/O BUS	A1U56-13, 14, 17, 18	3309780	11D6
I/O BUS	A1U45-09*	3309780	7D7
I/O BUS	A1U97-12	3309780	11C1
I/O BUS	A1U64-12*	3309780	7C5
I/O BUS	A1U42-03*	3309780	7C4
I/O BUS	A1U42-04*	3309780	7C4
I/O BUS	A1U41-14*	3309780	7D4

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
I/O BUS	A1U41-04*	3309780	7D4
I/O BUS	A1U43-14*	3309780	7C4
I/O BUS	A1U45-05*	3309780	7D7
I/O BUS	A1U87-06*	3309780	7B7
I/O BUS	A1U19-15*	3309780	7C3
I/O BUS	A1U41-13*	3309780	7D4
I/O BUS	A1U87-15*	3309780	7B7
I/O BUS	A1U87-16*	3309780	7B7
I/O BUS	A1U19-10*	3309780	7C3
I/O BUS	A1U19-09*	3309780	7C3
I/O BUS	A1U44-19*	3309780	7C7
I/O BUS	A1U87-12*	3309780	7B7
I/O BUS	A1U41-07*	3309780	7D4
I/O BUS	A1U19-01*	3309780	7C3
I/O BUS	A1U41-08*	3309780	7D4
I/O BUS	A1U45-02*	3309780	7D7
I/O BUS B0	A1U101-02	3309780	11A7
I/O BUS B1	A1U10-12	3309780	11A7
I/O BUS B5	A1U106-02	3309780	11B4
+INDEX	A5U5-01	3316180	4C7
+INDEX	A1U12-01	3309780	3B3
+INDEX	A1U93-08*	3309780	9B6
+INDEX	A1U7-01	3309780	3C8
+INDEX	A5J4-37	3316180	1C7
+INDEX	A5U33-07	3316180	4B3
+INDEX	A1J4-37	3309780	12C2
+INDEX	A1U100-03	3309780	11A7
+INDEX	A1U104-09	3309780	9B5
+INDEX BYTE TTL	A3U66-04	3309770	3A7
+INDEX BYTE TTL	A3U71-04*	3309770	2A5
+INDEX BYTE TTL	A3U61-12	3309770	3A5
-INDEX ENABLE	A1U53-10*	3309780	8C6
-INDEX ENABLE	A1U93-01	3309780	9B7
-INDEX ENABLE	A1U68-13	3309780	8C6
+INDEX FOUND	A1U99-04	3309780	11A6
+INDEX FOUND	A1U97-03	3309780	11C1
+INDEX FOUND	A1U100-05*	3309780	11A6
+INDEX FOUND	A1U111-05	3309780	11B7
+INDEX GATE (+INDEX GATE TTL)	A3U70-05*	3309770	3C4
+INDEX GATE TTL (+INDEX GATE)	A3U62-05	3309770	2A8
-INDEX RESET	A1U93-04	3309780	9B6
-INDEX RESET	A1U52-06*	3309780	8C7
-INITIALIZE	A1U73-12*	3309780	6A2
-INITIALIZE	A1U55-01	3309780	5C6
-INTERRUPT	A1U36-01	3309780	5B3
-INTERRUPT	A1U67-16	3309780	6C6
-INTERRUPT	A1U51-08*	3309780	5B3
+INWARD	A1U82-13*	3309780	10C5
+INWARD	A1U86-13	3309780	7D6
-IP10	A1U72-15*	3309780	6D2
-IP10	A1U45-01	3309780	7D7
-IP11	A1U72-14*	3309780	6D2

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-IP12	A1U85-01	3309780	7C7
-IP12	A1U72-13*	3309780	6D2
-IP13	A1U72-12*	3309780	6D2
-IP13	A1U87-01	3309780	7B7
-IP14	A1U86-01	3309780	7D6
-IP14	A1U72-11*	3309780	6C2
-IP15	A1U64-01	3309780	7C6
-IP15	A1U72-10*	3309780	6C2
-IP16	A1U72-09*	3309780	6C2
-IP16	A1U119-01	3309780	7C6
-IP17	A1U97-01	3309780	11C1
-IP17	A1U72-07*	3309780	6C2
+KEY 1	A1U119-03	3309780	7C6
+KEY 1	A1U120-17*	3309780	10B6
+KEY 2	A1U119-04	3309780	7C6
+KEY 2	A1U120-16*	3309780	10B6
+KEY 4	A1U119-07	3309780	7B6
+KEY 4	A1U120-15*	3309780	10B6
+KEY 8	A1U120-14*	3309780	10B6
+KEY 8	A1U119-08	3309780	7B6
-LOCK ON	A3U24-13	3309770	5D3
-LOCK ON	A3U18-05	3309770	6A4
-LOCK ON	A3J3-22	3309770	6A8
-LOCK ON	A1U41-09*	3309780	7D4
-LOCK ON	A3U25-13	3309770	6A6
-LOCK ON	A1J5-22	3309780	12C7
-LOCK ON	A3U5-16,01	3309770	6B2
-M VEL (-MED VEL)	A3U44-03	3309770	5A6
-M VEL (-MED VEL)	A3J3-10	3309770	5B1
-M VEL (-MED VEL)	A3U44-03	3309770	5A6
-M VEL (-MED VEL)	A3U54-05	3309770	4C8
-M VEL (-MED VEL)	A3U66-13*, -14*	3309770	5A2
-M VEL (-MED VEL)	A3U65-08, -16	3309770	5B7
-M VEL (-MED VEL)	A3U65-16,08	3309770	5B7
-M VEL (-MED VEL)	A3U66-13*,14*	3309770	5B2
MARS UNSAFE	A2U51-06	3309760	2B6
MARS UNSAFE	A2J2-25	3309760	2A8
MARS UNSAFE	A7J1-25*	3309800	1B3
+MCS (+MSC)	A2U51-14*	3309760	2A5
-MED VEL (-M VEL)	A1J5-10	3309780	12C7
-MED VEL (-M VEL)	A1U83-02	3309780	7A5
-MODULE 1	A2J2-17	3309760	1A8
-MODULE 1	A1U64-03	3309780	7C6
-MODULE 1	A7J1-17	3309800	1C3
-MODULE 1	A1J6-30	3309780	12C5
-MODULE 1	A7JUMPER-01*	3309800	1A5
-MODULE 1	A2J1-30	3309760	1A8
-MODULE 2	A1J6-29	3309780	12C5
-MODULE 2	A2J2-19	3309760	1A8
-MODULE 2	A7JUMPER-02*	3309800	1A5

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-MODULE 2	A2J1-29	3309760	1A8
-MODULE 2	A1U64-04	3309780	7C6
MODULE 2	A7J1-19	3309800	1C3
MODULE 4	A7J1-15	3309800	1C3
-MODULE 4	A2J2-15	3309760	1A8
-MODULE 4	A7JUMPER-04*	3309800	1A5
-MODULE 4	A2J1-28	3309760	1A8
-MODULE 4	A1U64-07	3309780	7C6
-MODULE 4	A1J6-28	3309780	12C5
-MODULE 8	A2J2-13	3309760	1A8
-MODULE 8	A7JUMPER-08*	3309800	1A5
-MODULE 8	A1J6-26	3309780	12C5
-MODULE 8	A2J1-26	3309760	1A8
-MODULE 8	A1U64-08	3309780	7C6
MODULE 8	A7J1-13	3309800	1C3
MOTOR DRIVE	A6J5-04	3309790	3D8
MOTOR DRIVE	A6K1-05	3309790	3D5
MOTOR DRIVE	A3J2-04*	3309770	7C3
MOTOR HI	A6K1-04*	3309790	3D3
MOTOR HI	A6J3-01	3309790	3D3
MOTOR LO	A6J3-02	3309790	3D3
+MOVE OUT	A3U27-10	3309770	6A2
+MOVE OUT	A3U43-01	3309770	5D5
+MOVE OUT	A3U25-08*	3309770	5D5
-MOVE OUT	A3U3-08,09	3309770	6D4
-MOVE OUT	A3J3-24	3309770	6C8
-MOVE OUT	A3U25-09	3309770	5D6
-MOVE OUT	A1J5-24	3309780	12D7
-MOVE OUT	A1U41-05*	3309780	7D4
-MOVE OUT	A3U27-12	3309770	6A2
+MSC (+MCS)	A2U40-02	3309760	1B5
+MSC (+MCS)	A2U50-01	3309760	1A5
MTR I FDBK	A6J5-02*	3309790	3D3
-MULTI CHIP SEL (-GATED MULT HD)	A1U77-12	3309780	10C4
-MULTI CHIP SEL (-GATED MULT HD)	A1J6-24	3309780	12C5
-MULTI CHIP SEL (-GATED MULT HD)	A1U85-13	3309780	7B7
NP	A3R160	3309770	5B7
NP	A3R210	3309770	5B7
NP	A3U54-09	3309770	5C7
NP	A3R93	3309770	5D8
NP	A3R209	3309770	5A7
NP	A3U53-07*	3309770	4A3
NP	A3U35-14	3309770	6B7
NP	A3U50-07*	3309770	4B2
NP	A3U35-06	3309770	6B7
NP XING	A3U55-07*, -12*	3309770	4A1
+NP XING	A3U46-12	3309770	5A6
+ODD HEAD	A1U63-03	3309780	5C6
+ODD HEAD	A1U42-06*	3309780	7C4
-OFFSET	A1J5-14	3309780	12C7
-OFFSET	A1U41-06*	3309780	7D4
-OFFSET	A3J3-14	3309770	6C7

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-OFFSET	A3U24-01	3309770	6A7
-OFFSET	A3U5-09	3309770	6C5
+OFFSET FORWARD	A1U36-08*	3309780	5B6
+OFFSET FORWARD	A1U64-17	3309780	7C6
+OFFSET FORWARD	A1U38-11	3309780	5B4
+OFFSET FORWARD	A1U34-03	3309780	5B6
+OFFSET REVERSE	A1U38-03	3309780	5B4
+OFFSET REVERSE	A1U36-11*	3309780	5B6
+OFFSET REVERSE	A1U34-02	3309780	5B6
+OFFSET REVERSE	A1U64-18	3309780	7C6
-OFFSET SELECT	A1U84-02	3309780	10D6
-OFFSET SELECT	A1U34-01*	3309780	5B5
+OGB #1	A1U60-10*	3309780	8C3
+OGB #1	A1U86-03	3309780	7D6
+OGB #2	A1U86-04	3309780	7D6
OGB #2	A1U60-06*	3309780	8B3
+ON CYLINDER	A1U18-10	3309780	10C3
+ON CYLINDER	A1U7-07	3309780	3D8
+ON CYLINDER	A1J4-38	3309780	12C2
+ON CYLINDER	A5J4-38	3316180	1C7
+ON CYLINDER	A1U36-03*	3309780	5B3
+ON CYLINDER	A1U25-06	3309780	4A3
+ON CYLINDER	A5U25-06	3316180	5A2
+ON CYLINDER	A5U5-07	3316180	4C7
+ON TRACK	A1U41-12*	3309780	7D4
+ON TRACK	A1U36-02	3309780	5B3
-OP20	A1U70-15*	3309780	6C2
-OP20	A1U41-11	3309780	7D4
-OP21	A1U42-11	3309780	7C4
-OP21	A1U70-14*	3309780	6C2
-OP22	A1U70-13*	3309780	6C2
-OP22	A1U43-11	3309780	7C4
-OP23	A1U70-12*	3309780	6C2
-OP23	A1U19-11	3309780	7B3
-OP24	A1U30-11	3309780	7D4
-OP24	A1U31-11	3309780	7C3
-OP24	A1U70-11*	3309780	6C2
-OP25	A1U70-10*	3309780	6C2
-OP25	A1U122-03*	3309780	10A3
-OP25	A1U123-03*	3309780	10A3
-OP26	A1U124-03	3309780	10A4
-OP26	A1U70-09*	3309780	6C2
-OP26	A1U121-03	3309780	10A5
-OP40	A1U73-15*	3309780	6B2
-OP40	A1U46-11	3309780	11D7
-OP41	A1U56-11	3309780	11D6
-OP41	A1U73-14*	3309780	6B2
-OP42	A1U50-11	3309780	11D5
-OP42	A1U73-13*	3309780	6B2
-OP43	A1U71-12*	3309780	6B2
OP43	A1U113-11	3309780	11B6

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-OP44	A1U101-03	3309780	11A7
-OP44	A1U73-11*	3309780	6B2
-OP44	A1U106-03	3309780	11B4
-OP45	A1U73-10*	3309780	6B2
-OP45	A1U35-11	3309780	11D3
-OPEN CABLE DETECT	A1U10-03	3309780	4C6
-OPEN CABLE DETECT	A1U59-12*	3309780	1B5
+OPEN CABLE DETECT	A5U16-04	3316180	2C5
+OPEN CABLE DETECT	A5U15-03*	3316180	2B5
+OPEN CABLE DETECT	A5U23-13	3316180	2B4
+OPEN CABLE DETECT	A5U27-09	3316180	5B7
-OUTER TRACK	A1U42-12*	3309780	7C4
-OUTER TRACK	A2J1-27	3309760	4A8
-OUTER TRACK	A2U64-04	3309760	4A8
-OUTER TRACK	A1J6-27	3309780	12C5
OUTPUT +(SERVO-X)	A7J1-28*	3309800	1B2
OUTPUT -(SERVO-Y)	A7J1-27*	3309800	1B2
+OUTWARD	A1U82-14*	3309780	10B5
+OUTWARD	A1U86-14	3309780	7D6
-PLO	A3J3-16	3309770	2B1
-PLO	A1J5-16	3309780	12D7
-PLO	A3U25-02*	3309770	2B1
-PLO (9.67 MHZ)	A1U40-17	3309780	3D5
+PLO LOCKED TTL	A3U61-05*	3309770	3B4
+PLO LOCKED TTL	A3U76-04,13	3309770	3C4
+PLO LOCKED TTL	A3U78-10,01	3309770	3D4
+PLO LOCKED TTL	A3U48-07	3309770	2C8
+PLO UNSAFE (+PLO UNSAFE TTL)	A1U74-03	3309780	10D7
+PLO UNSAFE (+PLO UNSAFE TTL)	A1J6-10	3309780	12C5
+PLO UNSAFE (+PLO UNSAFE TTL)	A1J5-07	3309780	12D7
+PLO UNSAFE TTL (+PLO UNSAFE)	A3J3-07	3309770	3B4
+PLO UNSAFE TTL (+PLO UNSAFE)	A3U81-01	3309770	2C5
+PLO UNSAFE TTL (+PLO UNSAFE)	A3U61-06*	3309770	3B4
+PLO UNSAFE TTL (+PLO UNSAFE)	A3U86-01	3309770	3A6
-POWER FAIL (-PWR FAIL)	A1U87-13	3309780	7B7
-POWER FAIL (-PWR FAIL)	A1U77-13	3309780	10C4
-POWER FAIL (-PWR FAIL)	A1J9-08	3309780	1C4
-POWER FAIL (-PWR FAIL)	A1U94-10	3309780	6B6
-POWER FAIL (-PWR FAIL)	A1U67-17	3309780	6B6
-POWER FAIL (-PWR FAIL)	A1U85-17	3309780	7B7
-POWER ON RESET	A3U89-01	3309770	3B6
-POWER ON RESET	A1U77-02	3309780	10C4
-POWER ON RESET	A1U43-01	3309780	7B4
-POWER ON RESET	A3U87-01	3309770	3B6
-POWER ON RESET	A3J3-01	3309770	3B8
-POWER ON RESET	A1U112-13	3309780	11B5
-POWER ON RESET	A1U42-01	3309780	7C4
-POWER ON RESET	A5U26-04	3316180	5B6
-POWER ON RESET	A1U41-01	3309780	7C4
-POWER ON RESET	A1J4-59	3309780	12B2
-POWER ON RESET	A1J5-01	3309780	12D7
-POWER ON RESET	A1U36-05	3309780	4C5

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-POWER ON RESET	A5U26-10	3316180	5C6
-POWER ON RESET	A5J4-59	3316180	1A7
-POWER ON RESET	A5U18-02	3316180	5B7
POWER ON RESET	A1U67-26	3309780	6A6
POWER ON RESET	A1U114-10*	3309780	6A6
-PWR FAIL (-POWER FAIL)	A6U7-08*	3309790	3A4
-PWR FAIL (-POWER FAIL)	A6J4-11	3309790	3A4
+QP	A3U47-05, 10	3309770	4D2
QP	A3U52-01*	3309770	4D3
QP	A3R120	3309770	5C8
QP	A3C90	3309770	5B8
QP	A3U50-01*	3309770	4C2
QP	A3U35-03	3309770	6B7
QP	A3R121	3309770	5D8
QP	A3U35-11	3309770	6B7
+QP XING	A3U46-13	3309770	5A6
+QP XING	A3U47-07*	3309770	4B1
+R/W UNSAFE	A2U40-04	3309760	1B5
+R/W UNSAFE	A251-01*	3309760	2B5
+R/W UNSAFE	A2U50-04	3309760	1B4
-R/W UNSAFE (-GATED R/W UNSAFE)	A1U77-10	3309780	10C4
-R/W UNSAFE (-GATED R/W UNSAFE)	A1U85-14	3309780	7B7
-R/W UNSAFE (-GATED R/W UNSAFE)	A1J6-16	3309780	12C5
-RAW READ DATA	A2U26-04	3309760	5A7
-RAW READ DATA	A2U56-10*	3309760	1C4
-RAW READ DATA	A2U36-04	3309760	5A7
+RAW READ DATA	A2U26-05	3309760	5A7
+RAW READ DATA	A2U36-07	3309760	5A8
+RAW READ DATA	A2U41-06	3309760	3C7
+RAW READ DATA	A2U56-11*	3309780	1C4
+RAW READ DATA	A2U29-06	3309760	3C7
+RD ERROR	A1U98-09*	3309780	11C2
+RD GATE (+READ GATE)	A2U38-05	3309760	2B2
+RD GATE (+READ GATE)	A2U44-06	3309760	2B7
-RD ONLY LED (-READ ONLY LED)	A1J8-39	3309780	12A4
-RD ONLY LED (-READ ONLY LED)	A1U114-12*	3309780	10B1
+READ	A1U108-02	3309780	11A4
+READ	A1U110-13	3309780	11B7
+READ	A1U100-09*	3309780	11A4
-READ CLOCK	A1U40-08	3309780	3B5
-READ CLOCK	A2J1-13	3309760	3A1
-READ CLOCK	A2U5-12*	3309760	3A3
-READ CLOCK	A1J6-13	3309780	12C5
-READ CLOCK BUF 1	A1U40-11	3309780	3B5
-READ CLOCK BUF 1	A1U40-12*	3309780	3B4
-READ CLOCK BUF 1	A1U74-13	3309780	11C8
-READ CLOCK BUF 2	A5U32-05	3316180	4C3
-READ CLOCK BUF 2	A5J4-06	3316180	1C7
-READ CLOCK BUF 2 (-CLOCK)	A1U40-09*	3309780	3B4
-READ CLOCK BUF 2 (-CLOCK)	A1U21-01	3309780	3B3
-READ CLOCK BUF 2 (-CLOCK)	A1J4-06	3309780	12D2
-READ DATA	A2U5-13*	3309760	3A3

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-READ DATA	A2J1-05	3309760	3A1
-READ DATA	A1J6-05	3309780	12C5
-READ DATA	A1U40-06	3309780	3B5
-READ DATA BUF 1	A1U40-13	3309780	3C5
-READ DATA BUF 1	A1U40-14*	3309780	3B4
-READ DATA BUF 1	A1U74-11	3309780	11C4
-READ DATA BUF 2	A5U32-01	3316180	4C3
-READ DATA BUF 2	A5J4-05	3316180	1C7
-READ DATA BUF 2 (-DATA)	A1U21-06	3309780	3C3
-READ DATA BUF 2 (-DATA)	A1U40-07*	3309780	3C4
-READ DATA BUF 2 (-DATA)	A1J4-05	3309780	12D2
-READ GATE	A2U43-07	3309760	3B7
-READ GATE	A2U30-06	3309760	3B7
-READ GATE	A2U43-01*	3309760	3B7
-READ GATE	A1U84-04	3309780	10D6
-READ GATE	A2U29-12	3309760	3B7
-READ GATE	A2U47-05	3309760	5B7
-READ GATE	A2J1-25	3309760	3B7
-READ GATE	A1U37-08*	3309780	5C6
-READ GATE	A1J6-25	3309780	12C5
-READ GATE	A2U47-12	3309760	5B7
+READ GATE (+RD GATE)	A2U43-03*	3309760	3B7
-READ ONLY LED (-RD ONLY LED)	A4DS8-C	3310060	1B7
-READ ONLY LED (-RD ONLY LED)	A4J1-39	3310060	1C7
-READ ONLY SW	A4S3*	3310060	1B7
-READ ONLY SW	A1J8-44	3309780	12C4
-READ ONLY SW	A1U84-03	3309780	10D6
-READ ONLY SW	A1U95-09	3309780	10B2
-READ ONLY SW	A4J1-44	3310060	1B7
+READY	A1U17-01	3309780	10D2
+READY	A1U41-15*	3309780	7C4
-READY LED	A1J8-41	3309780	12B4
-READY LED	A4J1-41	3310060	1C7
-READY LED	A1U114-06*	3309780	10C1
-READY LED	A4DS6-C	3310060	1C7
+RELAY DRIVE	A6DS4-A	3309790	3A4
+RELAY DRIVE	A6J2-05	3309790	3B4
+RELAY DRIVE	A6DS3-A	3309790	3B4
+RELAY DRIVE	A6DS1-A	3309790	3B4
+RELAY DRIVE	A6DS2-A	3309790	3B4
-RESET	A1U112-11*	3309780	11B5
-RESET	A1U101-01	3309780	11A7
-RESET	A1U10-13	3309780	11A7
-RESET GB ERROR	A1U68-12	3309780	8D4
-RESET GB ERROR	A1U76-10	3309780	8C6
-RESET GB ERROR	A1U71-11*	3309780	6A2
-RESET INTERRUPT	A1U38-04	3309780	5B4
-RESET INTERRUPT	A1U39-04	3309780	5C4
-RESET INTERRUPT	A1U38-10	3309780	5B4
-RESET INTERRUPT	A1U71-13*	3309780	6A2
-RESET INTERRUPT	A1U39-10	3309780	5A4

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-RESET UNSAFE	A1U71-14*	3309780	6B2
-RESET UNSAFE	A1U77-01	3309780	10C4
-REZERO	A1U59-10*	3309780	7C3
-REZERO	A3U33-09	3309770	6C5
-REZERO	A3U81-03	3309770	5C7
-REZERO	A3J3-25	3309770	5C8
-REZERO	A1J5-25	3309780	12B7
+REZERO INT	A1U64-14	3309780	7C6
+REZERO INT	A1U39-06*	3309780	5C4
-ROW Y1	A1U120-01	3309780	10B7
-ROW Y1	A4KEYBD-05*	3310060	1A7
-ROW Y1	A4J1-08	3310060	1B7
-ROW Y1	A1J8-08	3309780	12C4
-ROW Y2	A1U120-02	3309780	10A7
-ROW Y2	A1J8-07	3309780	12C4
-ROW Y2	A4KEYBD-06*	3310060	1A7
-ROW Y2	A4J1-07	3310060	1B7
-ROW Y3	A1U120-03	3309780	10A7
-ROW Y3	A4J1-06	3310060	1A7
-ROW Y3	A1J8-06	3309780	12C4
-ROW Y3	A4KEYBD-07*	3310060	1A7
-ROW Y4	A4J1-05	3310060	1A7
-ROW Y4	A1J8-05	3309780	12C4
-ROW Y4	A1U120-04	3309780	10A7
-ROW Y4	A4KEYBD-08*	3310060	1A7
-RUN	A3U34-01	3309770	6A8
-RUN	A6U8-06	3309790	3D6
-RUN	A6U10-06	3309790	3C7
-RUN	A3U44-05	3309770	5C6
-RUN	A3J3-23	3309770	7C8
-RUN	A3U33-08	3309770	7C7
-RUN	A6J4-09	3309790	3D7
-RUN	A1J9-06	3309780	1D2
-RUN	A1U69-12*	3309780	7C4
-RUN	A1J5-23	3309780	12B7
-RUN	A6U11-01	3309790	3B7
+RUN	A1U52-09	3309780	8D7
+RUN	A1U42-19*	3309780	7C4
-RUN RELAY DRIVE	A6J2-03	3309790	3B3
-RUN RELAY DRIVE	A6U11-03*	3309790	3B7
+SECTOR PULSE	A5J4-44	3316180	1B7
+SECTOR PULSE	A1U8-07	3309780	3A8
+SECTOR PULSE	A5U33-01	3316180	4B3
+SECTOR PULSE	A1U95-04*	3309780	9A4
+SECTOR PULSE	A1U12-07	3309780	3B3
+SECTOR PULSE	A1J4-44	3309780	12C2
+SECTOR PULSE	A5U6-01	3316180	4B7
+SEEK INCOMPLETE	A1U39-12	3309780	5A4
+SEEK INCOMPLETE	A1U7-15	3309780	3D8
+SEEK INCOMPLETE	A1U38-12	3309780	5C4
+SEEK INCOMPLETE	A1U16-01	3309780	10C3
+SEEK INCOMPLETE	A1U41-19*	3309780	7C4

TERM	ASSY/ COMPONENT/PIN	SCHM. DIAGRAM	SHEET COORD.
+SEEK INCOMPLETE	A1J4-36	3309780	12C2
+SEEK INCOMPLETE	A5U5-15	3316180	4D7
+SEEK INCOMPLETE	A1U38-02	3309780	5B4
+SEEK INCOMPLETE	A5J4-36	3316180	1C7
+SEEK INT	A1U39-08*	3309780	5A4
+SEEK INT	A1U64-13	3309780	7C6
-SELECT LED (-SELECTED LED)	A1U114-02*	3309780	10B1
-SELECT LED (-SELECTED LED)	A1J8-40	3309780	12A4
-SELECT SW0	A1U10-09	3309780	4C6
-SELECT SW0	A5U17-09	3316180	5B7
-SELECT SW0	A5J4-48	3316180	1B7
-SELECT SW0	A1S4-01*	3309780	4C7
-SELECT SW0	A1J4-48	3309780	12C2
-SELECT SW0	A1RP21-02	3309780	4C7
-SELECT SW1	A1U10-11	3309780	4C6
-SELECT SW1	A5J4-47	3316180	1B7
-SELECT SW1	A1J4-47	3309780	12C2
-SELECT SW1	A1S4-02*	3309780	4C7
-SELECT SW1	A1RP21-03	3309780	4C7
SELECT SW1	A5U17-11	3316180	5B7
SELECT SW2	A5U17-14	3316180	5B7
-SELECT SW2	A1RP21-04	3309780	4C7
-SELECT SW2	A5J4-50	3316180	1B7
-SELECT SW2	A1S4-03*	3309780	4C7
-SELECT SW2	A1J4-50	3309780	12C2
-SELECT SW2	A1U10-14	3309780	4C6
-SELECT SW3	A1J4-49	3309780	12C2
-SELECT SW3	A1S4-04*	3309780	4C7
-SELECT SW3	A1RP21-05	3309780	4C7
-SELECT SW3	A1U10-01	3309780	4C6
-SELECT SW3	A5J4-49	3316180	1B7
SELECT SW3	A5U17-01	3316180	5B7
-SELECTED LED	A4DS5-C	3310060	1C7
-SELECTED LED (-SELECT LED)	A4J1-40	3310060	1C7
-SEQUENCE HOLD	A1U87-04	3309780	7B7
-SEQUENCE HOLD	A1U29-12*, A1U29-07	3309780	4B6
-SEQUENCE PICK	A1U87-03	3309780	7B7
-SEQUENCE PICK	A1U29-02*, A1U29-14	3309780	4A6
+SERVO BITS	A3U68-03,06	3309770	4A7
+SERVO BITS	A3Q6E*	3309770	1C5
-SERVO CLOCK	A1J5-09	3309780	12C7
-SERVO CLOCK (+SERVO CLOCK TTL)	A1U52-08	3309780	8D7
-SERVO CLOCK (+SERVO CLOCK TTL)	A1U27-01	3309780	8C7
+SERVO CLOCK TTL	A3U62-07	3309770	2A8
+SERVO CLOCK TTL (+SERVO CLOCK)	A3U77-14	3309770	3C5
+SERVO CLOCK TTL (+SERVO CLOCK)	A3U87-02	3309770	3B6
+SERVO CLOCK TTL (+SERVO CLOCK)	A3U44-03	3309770	3A4
+SERVO CLOCK TTL (+SERVO CLOCK)	A3U89-02	3309770	3B6
+SERVO CLOCK TTL (+SERVO CLOCK)	A3U79-11*	3309770	3C6
+SERVO CLOCK TTL (+SERVO CLOCK)	A3U61-03,11	3309770	3B4
-SERVO CLOCK TTL (+SERVO CLOCK)	A3J3-09	3309770	3A3
-SERVO CLOCK TTL (+SERVO CLOCK)	A3U44-08*	3309770	3A3

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-SERVO DISABLE	A1U41-16*	3309780	7C4
-SERVO DISABLE	A1J5-11	3309780	12C7
-SERVO DISABLE	A3J3-11	3309770	7C8
-SERVO DISABLE	A3U33-01,16	3309770	7C7
SERVO GROUND	A7J1-29,30,33,34	3309800	1B3
+SERVO ONE BYTE	A3U61-08*	3309770	3A4
+SERVO ONE BYTE (+SERVO ONE BYTE TTL)	A1U52-01	3309780	8D7
+SERVO ONE BYTE (+SERVO ONE BYTE TTL)	A1J5-05	3309780	12C7
SERVO ONE BYTE TTL (+SERVO ONE BYTE)	A3J3-05	3309770	3A4
+SERVO SQUARE BITS (SQUARED SERVO BITS)	A1J5-03	3309780	12C7
-SERVO SQUARE BITS (SQUARED SERVO BITS)	A1U106-11	3309780	8B6
-SERVO SQUARE BITS (SQUARED SERVO BITS)	A1U92-12	3309780	8B6
SERVO VOLTAGE	A3R23	3309770	7C3
SERVO VOLTAGE	A1CR9	3309780	10C7
SERVO VOLTAGE	A3J3-02*	3309770	7C3
SERVO VOLTAGE	A1J5-02	3309780	12C7
SERVO VOLTAGE	A1CR8	3309780	10B7
SERVO-X (OUTPUT+)	A3J4-02	3309770	1C8
SERVO-X (OUTPUT+)	A3L10	3309770	1C8
SERVO-Y (OUTPUT-)	A3L9	3309770	1C8
SERVO-Y (OUTPUT-)	A3J4-01	3309770	1C8
-SET UNSAFE	A1U76-03	3309780	10D4
-SET UNSAFE	A1U71-15*	3309780	6B2
+SPLIT FIELD	A1U63-01	3309780	5C5
+SPLIT FIELD	A1U42-09*	3309780	7C4
SQUARED SERVO BITS	A3U80-04*	3309770	1C3
SQUARED SERVO BITS	A3U44-11	3309770	1C2
SQUARED SERVO BITS	A3U48-05	3309770	2C8
-SQUARED SERVO BITS(-SERVO SQUARE BITS)	A3J3-03	3309770	1C2
-SQUARED SERVO BITS(-SERVO SQUARE BITS)	A3U44-10*	3309770	1C2
-START	A1J9-07	3309780	1D3
-START	A1U69-10*	3309780	7C3
-START RELAY DRIVE	A6J2-04	3309790	3B3
-START RELAY DRIVE	A6U11-05*	3309790	3B7
-STROBE EARLY	A2U43-10	3309760	3D8
-STROBE EARLY	A1J6-19	3309780	12C5
-STROBE EARLY	A1U33-08*	3309780	5B6
-STROBE EARLY	A2J1-19	3309760	3D8
-STROBE LATE	A2U43-11	3309760	3D8
-STROBE LATE	A1U33-03*	3309780	5A6
-STROBE LATE	A1J6-21	3309780	12C5
-STROBE LATE	A2J1-21	3309760	3D8
-SYNC BYTE TTL	A3U86-13	3309770	3A6
-SYNC BYTE TTL	A3U71-05*	3309770	2B6
-SYNC BYTE TTL	A3U87-09	3309770	3B7
+SYNC ERROR	A1U97-13	3309780	11C1
+SYNC ERROR	A1U98-05*	3309780	11A4
+SYNC FOUND	A1U109-05	3309780	11C6
+SYNC FOUND	A1U97-07	3309780	11C1
+SYNC FOUND	A1U108-05*	3309780	11A4
+SYNC FOUND	A1U109-12	3309780	11C4

TERM	ASSY/ COMPONENT/PIN	SCHM. DIAGRAM	SHEET COORD.
+SYNC GATE TTL	A3U48-10	3309770	2B8
+SYNC GATE TTL	A3U70-09*	3309770	3B4
TABY-N	A1U20-12*	3309780	3D2
TABY-N	A1J2-21	3309780	3D2
TABY-N	A1J1-21	3309780	3D2
TABY-P	A1U20-13*	3309780	3D2
TABY-P	A1J2-51	3309780	3D2
TABY-P	A1J1-51	3309780	3D2
TACH A	A3R90	3309770	6C4
TACH-A	A3R212	3309770	5B3
TACH-A	A3U64-07*	3309770	5C3
TACT-P	A1J2-47	3309780	3C6
TACY-N	A1J1-17	3309780	3C6
TACY-N	A1J2-17	3309780	3C6
TACY-N	A1U7-04*	3309780	3C7
TACY-P	A1J1-47	3309780	3C6
TACY-P	A1U7-05*	3309780	3C7
TAFT-N	A1J1-15	3309780	3D6
TAFT-N	A1J2-15	3309780	3D6
TAFT-N	A1U7-12*	3309780	3D7
TAFT-P	A1U7-11*	3309780	3D7
TAFT-P	A1J2-45	3309780	3D6
TAFT-P	A1J1-45	3309780	3D6
TAIN-N	A1U7-03*	3309780	3C7
TAIN-N	A1J1-18	3309780	3C6
TAIN-N	A1J2-18	3309780	3C6
TAIN-P	A1U7-02*	3309780	3C7
TAIN-P	A1J2-48	3309780	3C6
TAIN-P	A1J1-48	3309780	3C6
TAMK-N	A1J1-20	3309780	3B6
TAMK-N	A1J2-20	3309780	3B6
TAMK-N	A1U8-14*	3309780	3B7
TAMK-P	A1J2-50	3309780	3B6
TAMK-P	A1J1-50	3309780	3B6
TAMK-P	A1U8-13*	3309780	3B7
TARD-N	A1U8-12*	3309780	3B7
TARD-N	A1J1-19	3309780	3B6
TARD-N	A1J2-19	3309780	3B6
TARD-P	A1U8-11*	3309780	3B7
TARD-P	A1J1-49	3309780	3B6
TARD-P	A1J2-49	3309780	3B6
TASC-N	A1J2-25	3309780	3B6
TASC-N	A1J1-25	3309780	3B6
TASC-N	A1U8-04*	3309780	3B7
TASC-P	A1J1-55	3309780	3A6
TASC-P	A1U8-05*	3309780	3A7
TASC-P	A1J2-55	3309780	3A6
TASE-N	A1U7-13*	3309780	3D7
TASE-N	A1J1-16	3309780	3D6
TASE-N	A1J2-16	3309780	3D6

TKRM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
TASE-P	A1J1-46	3309780	3D6
TASE-P	A1U7-14*	3309780	3D7
TASE-P	A1J2-46	3309780	3D6
TAWP-N	A1J2-28	3309780	3A6
TAWP-N	A1U8-03*	3309780	3A7
TAWP-N	A1J1-28	3309780	3A6
TAWP-P	A1J2-58	3309780	3A6
TAWP-P	A1U8-02*	3309780	3A7
TAWP-P	A1J1-58	3309780	3A6
TBBY-N	A5U31-12*	3316180	4D3
TBBY-N	A5J1-21*, A5J2-21	3316180	4D2
TBBY-P	A5U31-13*	3316180	4D3
TBBY-P	A5J1-51*, A5J2-51	3316180	4D2
TBCK-N	A5U5-05*	3316180	4C7
TBCK-N	A5J2-17	3316180	4C5
TBCK-N	A5J1-17*, A5J2-17	3316180	4C5
TBCK-P	A5J1-47*, A5J2-47	3316180	4C5
TBCK-P	A5U5-04*	3316180	4C6
TBFT-N	A5J2-15	3316180	4D5
TBFT-N	A5U5-12*	3316180	4D7
TBFT-N	A5J1-15*	3316180	4D5
TBFT-P	A5J1-45*, A5J2-45	3316180	4D5
TBFT-P	A5U5-11*	3316180	4D7
TBFT-P	A5J2-45	3316180	4D5
TBIN-N	A5U5-03*	3316180	4C6
TBIN-N	A5J1-18*, A5J2-18	3316180	4C5
TBIN-P	A5J1-48*, A5J2-48	3316180	4C5
TBIN-P	A5U5-02*	3316180	4C6
TBMK-N	A5U6-11*	3316180	4B6
TBMK-N	A5J1-20*, A5J2-20	3316180	4B5
TBRD-N	A5U6-13*	3316180	4B6
TBRD-N	A5J1-19*, A5J2-19	3316180	4B5
TBRD-P	A5J1-49*, A5J2-49	3316180	4B5
TBRD-P	A5U6-14*	3316180	4B6
TBSC-N	A5J1-25*, A5J2-25	3316180	4B5
TBSC-P	A5J1-55*, A5J2-55	3316180	4B5
TBSE-N	A5J1-16*	3316180	4C5
TBSE-N	A5U5-13*	3316180	4C7
TBSE-N	A5J2-16	3316180	4C5
TBSE-P	A5U5-14*	3316180	4C7
TBSE-P	A5J2-46	3316180	4C5
TBSE-P	A5J1-46*, A5J2-46	3316180	4C5
TBSO-N	A5U6-03*	3316180	4B6
TBSO-P	A5U6-02*	3316180	4B6
TBWP-N	A5U6-04*	3316180	4A6
TBWP-P	A5U6-05*	3316180	4A5
TBWP-P	A5J1-58*, A5J2-58	3316180	4A5
THRESHOLD	A2U53-13	3309760	1C7
THRESHOLD	A2U53-10	3309760	1C7
THRESHOLD	A2Q6C*	3309760	4C2

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-UNSAFE	A1U35-08*	3309780	10D3
-UNSAFE	A2U40-06	3309760	1C6
-UNSAFE	A2U39-12	3309760	1B5
-UNSAFE	A1U17-02	3309780	10D2
-UNSAFE	A1J6-03	3309780	12C5
-UNSAFE	A2U50-09	3309760	1B6
-UNSAFE	A2U59-13	3309760	2A4
-UNSAFE	A2J1-03	3309760	1B8
-UNSAFE	A1U18-09	3309780	10C2
-UNSAFE	A2U39-05	3309760	1B5
+UNSAFE	A5J4-35	3316180	1C7
+UNSAFE	A1U76-04*	3309780	10C3
+UNSAFE	A1J4-35	3309780	12C2
+UNSAFE	A1U87-08	3309780	7B7
+UNSAFE	A1U114-03	3309780	10C2
+UNSAFE	A5U5-10	3316180	4D7
+UNSAFE	A1U7-10	3309780	3D8
+UNSAFE	A2U39-11*	3309760	1B4
+UNSAFE	A1U35-09	3309780	10D3
+UNSAFE	A1U112-02	3309780	10C3
+UNSAFE CLOCK	A1U112-03*	3309780	10C1
-UNSAFE LED (-FAULT LED)	A1J8-43	3309780	12A4
-UNSAFE LED (-FAULT LED)	A1U114-04*	3309780	10C1
+UPSPEED	A1U92-06*	3309780	8B6
+UPSPEED	A1U87-07	3309780	7B7
+VCO TO (VFO TO)	A2U47-04	3309760	5B8
VEL COMP 1	A3U1-08	3309770	6D4
VEL COMP 2	A3U1-16	3309770	6D5
VELCOMP1	A3U27-08*	3309770	6A2
VELCOMP2	A3U27-05*	3309770	6A3
VFO TO (+VCO TO)	A2U20-03*	3309760	3C4
VFO TO (+VCO TO)	A2U13-02	3309760	3C4
+WRITE	A1U105-01	3309780	11B4
+WRITE	A1U110-01	3309780	11B7
+WRITE	A1U99-06*	3309780	11A5
+WRITE	A1U108-12	3309780	11B4
+WRITE	A1U22-13	3309780	11C2
-WRITE CLK (-WRITE CLOCK BUF)	A2U6-10	3309760	2D7
-WRITE CLK (-WRITE CLOCK BUF)	A2J1-15	3309760	2D7
-WRITE CLOCK	A1U22-08*	3309780	11A6
-WRITE CLOCK	A1J4-08	3309780	12C2
-WRITE CLOCK	A5U30-03*	3316180	3A2
-WRITE CLOCK	A1U11-05*	3309780	2A2
-WRITE CLOCK	A1U40-15	3309780	3C5
-WRITE CLOCK	A5J4-08	3316180	1D7
-WRITE CLOCK BUF (-WRITE CLK)	A1U40-05*	3309780	3C4
-WRITE CLOCK BUF (-WRITE CLK)	A1J6-15	3309780	12C5
WRITE CURRENT	A7J1-07	3309800	1D3
WRITE CURRENT	A2U66-07	3309760	4B5
WRITE CURRENT	A2Q9C*	3309760	4B6
WRITE CURRENT	A2J2-07	3309760	4B1

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-WRITE DATA	A1J4-09	3309780	12C2
-WRITE DATA	A2U6-07	3309760	2D7
-WRITE DATA	A5U30-05*	3316180	3A2
-WRITE DATA	A1U22-11*	3309780	11C2
-WRITE DATA	A5J4-09	3316180	1C7
-WRITE DATA	A1U40-04	3309780	3C5
-WRITE DATA	A1U11-03*	3309780	2B2
-WRITE DATA BUF	A1J6-01	3309780	12C5
-WRITE DATA BUF	A2J1-01	3309760	2D7
-WRITE DATA BUF	A1U40-16*	3309780	3C4
-WRITE ERROR	A1U85-08	3309780	7B7
-WRITE ERROR	A1U84-14*	3309780	10C6
-WRITE GATE	A2U39-01	3309760	1B5
-WRITE GATE	A1U37-06*	3309780	5C6
-WRITE GATE	A1J6-23	3309780	12C5
-WRITE GATE	A2U50-13	3309760	1B7
-WRITE GATE	A2J1-23	3309760	1B8
-WRITE GATE	A1U84-05	3309780	10D6
-WRITE MFM	A2U38-03*	3309760	2B2
-WRITE MFM	A2Q13B	3309760	4C7
+WRITE MFM	A2Q12B	3309760	4C7
+WRITE MFM	A2U38-02*	3309760	2B2
+WRITE PATTERN	A1U109-09	3309780	11C6
+WRITE PATTERN	A1U108-09*	3309780	11B4
+WRITE PROTECT	A1U95-08*	3309780	10B3
+WRITE PROTECT	A5J4-43	3316180	1B7
+WRITE PROTECT	A1U8-01	3309780	3A8
+WRITE PROTECT	A5U6-07	3316180	4A7
+WRITE PROTECT	A1J4-43	3309780	12C2
+WRITE SELECT (+WRITE SELECT)	A7J1-20	3309800	1C3
WRITE SELECT (+WRITE SELECT)	A2J2-20	3309760	4B1
WRITE SELECT (+WRITE SELECT)	A2Q14E*	3309760	4B4
->DIFF 256	A1J5-13	3309780	12C7
->DIFF 256	A1U30-12*	3309780	7D2

CONNECTOR-PIN/COMPONENT-PIN TERMS

This section includes an alpha-numeric listing of connector-pin and component-pin terms. Only pin terms that appear on the PCBA schematics are included in this list (e.g., d-c power pins are excluded). The intent of this list is to assist the user in determining the function of a specific connector/component pin. This list is intended for reference use only and is not intended to be used as a wire list. In some cases, identical terms are given different term names. In these cases, the alternate term name is also listed in parenthesis. See Figure 2.

NOTE

The origin(s) of each signal is denoted by an asterisk (*).

Capricorn assembly designations are as follows:

- A1 -- I/O Control PCBA (CTROL)
- A2 -- Read/Write PCBA (READW)
- A3 -- Servo Driver PCBA (SERDV)
- A4 -- Diagnostic Control PCBA (DICO2)
- A5 -- Dual Port PCBA (DUPOC)
- A6 -- Power Supply Regulator PCBA (REGUL)
- A7 -- HDA Interface PCBA (HDAIN)

ASSY/ COMPONENT/PIN	TERM	SCHM. DIAGRAM	SHEET COORD.
AlU4-04	- A PORT ENABLE	3309780	2A7
AlU40-02	- 9.67 CLOCK BUF 1	3309780	3D5
AlU40-03*	- 9.67 CLOCK BUF 1	3309780	3D5
AlU40-04	- WRITE DATA	3309780	3C5
AlU40-05*	- WRITE CLOCK BUF (-WRITE CLK)	3309780	3C4
AlU40-06	- READ DATA	3309780	3B5
AlU40-07*	- READ DATA BUF 2 (-DATA)	3309780	3C4
AlU40-08	- READ CLOCK	3309780	3B5
AlU40-09*	- READ CLOCK BUF 2 (-CLOCK)	3309780	3B4

PCBA

COMPONENT

PIN

INDICATES
SIGNAL
ORIGIN

ALPHA-NUMERIC TERM

SYMBOL INDICATES
POLARITY OF SIGNAL
WHEN ASSERTED
(ABSENCE OF SIGN
INDICATES POSITIVE
POLARITY)

IDENTICAL SIGNAL WITH
ALTERNATE TERM NAME
(SEE ALTERNATE TERM
NAME FOR REMAINING
SIGNAL DESTINATION(S)
OR ORIGIN(S).

SCHMATIC
DRAWING NO.

COORDINATES

SHEET NO.
OF DRAWING

Figure 2

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1CR4	-BHL 0	3309780	4A7
A1CR8	SERVO VOLTAGE	3309780	10B7
A1CR9	SERVO VOLTAGE	3309780	10C7
A1J1-01*	AFT1-N	3309780	2C4
A1J1-02*	AFT2-N	3309780	2C4
A1J1-03*	AFT3-N	3309780	2B4
A1J1-04*	ABS0-N	3309780	2D8
A1J1-05*	ABS1-N	3309780	2D8
A1J1-06*	ABS2-N	3309780	2C8
A1J1-07*	ABS3-N	3309780	2C8
A1J1-08*	ABS4-N	3309780	2B8
A1J1-09*	ABS5-N	3309780	2B8
A1J1-10*	ABS6-N	3309780	2B8
A1J1-11*	ABS7-N	3309780	2B8
A1J1-12*	ABS8-N	3309780	2D4
A1J1-13*	ABS9-N	3309780	1A8
A1J1-14*	ARDV-N	3309780	1C8
A1J1-15	TAFT-N	3309780	3D6
A1J1-16	TASE-N	3309780	3D6
A1J1-17	TACY-N	3309780	3C6
A1J1-18	TAIN-N	3309780	3C6
A1J1-19	TARD-N	3309780	3B6
A1J1-20	TAMK-N	3309780	3B6
A1J1-21	TABY-N	3309780	3D2
A1J1-22*	ARSL-N	3309780	1B8
A1J1-23*	ARSO-N	3309780	1D8
A1J1-24*	ARS1-N	3309780	1D8
A1J1-25	TASC-N	3309780	3B6
A1J1-26*	ARS2-N	3309780	1C8
A1J1-27*	ARS3-N	3309780	1C8
A1J1-28	TAWP-N	3309780	3A6
A1J1-29*	-ASQ 1	3309780	4A8
A1J1-30*	ABS10-N	3309780	2D4
A1J1-31*	AFT1-P	3309780	2C4
A1J1-32*	AFT2-P	3309780	2C4
A1J1-33*	AFT3-P	3309780	2B4
A1J1-34*	ABS0-P	3309780	2D8
A1J1-35*	ABS1-P	3309780	2D8
A1J1-36*	ABS2-P	3309780	2C8
A1J1-37*	ABS3-P	3309780	2C8
A1J1-38*	ABS4-P	3309780	2B8
A1J1-39*	ABS5-P	3309780	2B8
A1J1-40*	ABS6-P	3309780	2B8
A1J1-41*	ABS7-P	3309780	2A8
A1J1-42*	ABS8-P	3309780	2D4
A1J1-43*	ABS9-P	3309780	1A8
A1J1-44*	ARDV-P	3309780	1B8
A1J1-45	TAFT-P	3309780	3D6
A1J1-46	TASE-P	3309780	3D6
A1J1-47	TACY-P	3309780	3C6
A1J1-48	TAIN-P	3309780	3C6
A1J1-49	TARD-P	3309780	3B6
A1J1-50	TAMK-P	3309780	3B6
A1J1-51	TABY-P	3309780	3D2
A1J1-52*	ARSL-P	3309780	1A8

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1J1-53*	ARS0-P	3309780	1D8
A1J1-54*	ARS1-P	3309780	1C8
A1J1-55	TASC-P	3309780	3A6
A1J1-56*	ARS2-P	3309780	1C8
A1J1-57*	ARS3-P	3309780	1C8
A1J1-58	TAWP-P	3309780	3A6
A1J1-59*	-AHL 1	3309780	4A8
A1J1-60*	ABS10-P	3309780	2D4
A1J2-01	AFT1-N	3309780	2C4
A1J2-02	AFT2-N	3309780	2C4
A1J2-03	AFT3-N	3309780	2B4
A1J2-04	ABS0-N	3309780	2D8
A1J2-05	ABS1-N	3309780	2D8
A1J2-06	ABS2-N	3309780	2C8
A1J2-07	ABS3-N	3309780	2C8
A1J2-08	ABS4-N	3309780	2B8
A1J2-09	ABS5-N	3309780	2B8
A1J2-10	ABS6-N	3309780	2B8
A1J2-11	ABS7-N	3309780	2B8
A1J2-12	ABS8-N	3309780	2D4
A1J2-13	ABS9-N	3309780	1A7
A1J2-14	ARDV-N	3309780	1C7
A1J2-15	TAFT-N	3309780	3D6
A1J2-16	TASE-N	3309780	3D6
A1J2-17	TACY-N	3309780	3C6
A1J2-18	TAIN-N	3309780	3C6
A1J2-19	TARD-N	3309780	3B6
A1J2-20	TAMK-N	3309780	3B6
A1J2-21	TABY-N	3309780	3D2
A1J2-22	ARSL-N	3309780	1B7
A1J2-23	ARS0-N	3309780	1D7
A1J2-24	ARS1-N	3309780	1D7
A1J2-25	TASC-N	3309780	3B6
A1J2-26	ARS2-N	3309780	1C7
A1J2-27	ARS3-N	3309780	1C7
A1J2-28	TAWP-N	3309780	3A6
A1J2-29	-ASQ 0	3309780	4A1
A1J2-30	ABS10-N	3309780	2D4
A1J2-31	AFT1-P	3309780	2C4
A1J2-32	AFT2-P	3309780	2C4
A1J2-33	AFT3-P	3309780	2B4
A1J2-34	ABS0-P	3309780	2D8
A1J2-35	ABS1-P	3309780	2D8
A1J2-36	ABS2-P	3309780	2C8
A1J2-37	ABS3-P	3309780	2C8
A1J2-38	ABS4-P	3309780	2B8
A1J2-39	ABS5-P	3309780	2B8
A1J2-40	ABS6-P	3309780	2B8
A1J2-41	ABS7-P	3309780	2B8
A1J2-42	ABS8-P	3309780	2D4
A1J2-43	ABS9-P	3309780	1A7
A1J2-44	ARDV-P	3309780	1B7
A1J2-45	TAFT-P	3309780	3D6
A1J2-46	TASE-P	3309780	3D6
A1J2-47	TACT-P	3309780	3C6

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1J2-48	TAIN-P	3309780	3C6
A1J2-49	TARD-P	3309780	3B6
A1J2-50	TAMK-P	3309780	3B6
A1J2-51	TABY-P	3309780	3D2
A1J2-52	ARSL-P	3309780	1A7
A1J2-53	ARSO-P	3309780	1D7
A1J2-54	ARS1-P	3309780	1C7
A1J2-55	TASC-P	3309780	3A6
A1J2-56	ARS2-P	3309780	1C7
A1J2-57	ARS3-P	3309780	1C7
A1J2-58	TAWP-P	3309780	3A6
A1J2-59	-AHL 0	3309780	4A1
A1J2-60	ABS10-P	3309780	2D4
A1J3-01	ASCK-G	3309780	3C2
A1J3-02	ASCK-N	3309780	3C2
A1J3-03	ARDT-N	3309780	3C3
A1J3-04	ARCK-G	3309780	3B2
A1J3-05	ARCK-N	3309780	3B2
A1J3-06*	AWCK-N	3309780	2A4
A1J3-07	AWDT-G	3309780	2B4
A1J3-08*	AWDT-N	3309780	2B4
A1J3-09	ASEL-P	3309780	3B2
A1J3-10	ASKN-N	3309780	3B2
A1J3-12	AIDX-N	3309780	3B2
A1J3-13	ASCT-N	3309780	3A2
A1J3-14	ASCK-P	3309780	3C2
A1J3-15	ARDT-G	3309780	3C2
A1J3-16	ARDT-P	3309780	3C2
A1J3-17	ARCK-P	3309780	3B2
A1J3-18	AWCK-G	3309780	2A4
A1J3-19*	AWCK-P	3309780	2A4
A1J3-20*	AWDT-P	3309780	2B4
A1J3-22	ASEL-N	3309780	3B2
A1J3-23	ASKN-P	3309780	3B2
A1J3-24	AIDX-P	3309780	3A2
A1J3-26	ASCT-P	3309780	3A2
A1J4-01	-BHL1	3309780	12C2
A1J4-02	-BHLO	3309780	12B2
A1J4-03	-BSQ1	3309780	12C2
A1J4-04	-BSQ0	3309780	12B2
A1J4-05	-READ DATA BUF 2 (-DATA)	3309780	12D2
A1J4-06	-READ CLOCK BUF 2 (-CLOCK)	3309780	12D2
A1J4-07	-9.67 CLOCK BUF 2 (-9.67 CLK)	3309780	12D2
A1J4-08	-WRITE CLOCK	3309780	12C2
A1J4-09	-WRITE DATA	3309780	12C2
A1J4-10	-A CONTROL TAG	3309780	12C2
A1J4-11	-B BUS 8	3309780	12C2
A1J4-12	-B BUS 10	3309780	12C2
A1J4-13	-CYLINDER TAG	3309780	12C2
A1J4-14	-HEAD TAG (-HD TAG)	3309780	12C2
A1J4-15	-B BUS 1	3309780	12D2
A1J4-16	-B BUS 0	3309780	12D2
A1J4-17	-B BUS 2	3309780	12D2
A1J4-18	-B BUS 3	3309780	12C2
A1J4-19	-B BUS 5	3309780	12C2

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1J4-20	-B BUS 4	3309780	12C2
A1J4-21	-B BUS 6	3309780	12C2
A1J4-22	-B BUS 7	3309780	12C2
A1J4-23	-A BUS 9	3309780	12B2
A1J4-24	-B RELEASE	3309780	12B2
A1J4-25	-A RELEASE	3309780	12B2
A1J4-26	+A RESERVED	3309780	12C2
A1J4-27	-B SELECTED	3309780	12C2
A1J4-28	-A SELECTED	3309780	12B2
A1J4-29	-B BUS 9	3309780	12C2
A1J4-30	-DIAGNOSTICS	3309780	12B2
A1J4-31	-B RESERVED	3309780	12C2
A1J4-32	-4 MHZ CLOCK	3309780	12B2
A1J4-33	-A RAW SELECT	3309780	12B2
A1J4-34	-A INHIBIT	3309780	12C2
A1J4-35	+UNSAFE	3309780	12C2
A1J4-36	+SEEK INCOMPLETE	3309780	12C2
A1J4-37	+INDEX	3309780	12C2
A1J4-38	+ON CYLINDER	3309780	12C2
A1J4-39	+FILE READY	3309780	12C2
A1J4-40	-AM DETECTED	3309780	12C2
A1J4-42	-B CONTROL TAG	3309780	12B2
A1J4-43	+WRITE PROTECT	3309780	12C2
A1J4-44	+SECTOR PULSE	3309780	12C2
A1J4-47	-SELECT SW1	3309780	12C2
A1J4-48	-SELECT SW0	3309780	12C2
A1J4-49	-SELECT SW3	3309780	12C2
A1J4-50	-SELECT SW2	3309780	12C2
A1J4-59	-POWER ON RESET	3309780	12B2
A1J5-01	-POWER ON RESET	3309780	12D7
A1J5-02	SERVO VOLTAGE	3309780	12C7
A1J5-03	+SERVO SQUARE BITS (SQUARED SERVO BITS)	3309780	12C7
A1J5-04	DIFF 1024	3309780	12C7
A1J5-05	+SERVO ONE BYTE (+SERVO ONE BYTE TTL)	3309780	12C7
A1J5-06	-DIFF 256	3309780	12C7
A1J5-07	+PLO UNSAFE (+PLO UNSAFE TTL)	3309780	12D7
A1J5-08	-DIFF 512 (-512)	3309780	12C7
A1J5-09	-SERVO CLOCK	3309780	12C7
A1J5-10	-MED VEL (-M VEL)	3309780	12C7
A1J5-11	-SERVO DISABLE	3309780	12C7
A1J5-12	-CYL TRANS	3309780	12C7
A1J5-13	->DIFF 256	3309780	12C7
A1J5-14	-OFFSET	3309780	12C7
A1J5-15	-FINE TRACK	3309780	12C7
A1J5-16	-PLO	3309780	12D7
A1J5-17	+CAR 2	3309780	12C7
A1J5-19	+CAR 1	3309780	12C7
A1J5-20	-DIFF #0	3309780	12C7
A1J5-22	-LOCK ON	3309780	12C7
A1J5-23	-RUN	3309780	12B7
A1J5-24	-MOVE OUT	3309780	12D7
A1J5-25	-REZERO	3309780	12B7
A1J5-27	DIFF 128 (-128)	3309780	12C7
A1J5-28	-DIFF 64 (-64)	3309780	12C7
A1J5-29	-DIFF 8 (-8)	3309780	12C7

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1J5-30	-DIFF 32 (-32)	3309780	12C7
A1J5-31	-DIFF 4 (-4)	3309780	12C7
A1J5-32	-DIFF 16 (-16)	3309780	12C7
A1J5-33	-DIFF 2 (-2)	3309780	12C7
A1J5-34	-DIFF 1 (-1)	3309780	12C7
A1J6-01	-WRITE DATA BUF	3309780	12C5
A1J6-03	-UNSAFE	3309780	12C5
A1J6-05	-READ DATA	3309780	12C5
A1J6-09	-AM ENABLE (-ADDRESS MARK ENABLE)	3309780	12C5
A1J6-10	+PLO UNSAFE (+PLO UNSAFE TTL)	3309780	12C5
A1J6-13	-READ CLOCK	3309780	12C5
A1J6-14	-HD TAG (-HEAD TAG)	3309780	12C5
A1J6-15	-WRITE CLOCK BUF (-WRITE CLK)	3309780	12C5
A1J6-16	-R/W UNSAFE (-GATED R/W UNSAFE)	3309780	12C5
A1J6-17	AM DETECTED	3309780	12C5
A1J6-19	-STROBE EARLY	3309780	12C5
A1J6-21	-STROBE LATE	3309780	12C5
A1J6-23	-WRITE GATE	3309780	12C5
A1J6-24	-MULTI CHIP SEL (-GATED MULT HD)	3309780	12C5
A1J6-25	-READ GATE	3309780	12C5
A1J6-26	-MODULE 8	3309780	12C5
A1J6-27	-OUTER TRACK	3309780	12C5
A1J6-28	-MODULE 4	3309780	12C5
A1J6-29	-MODULE 2	3309780	12C5
A1J6-30	-MODULE 1	3309780	12C5
A1J6-31	-HAR 4	3309780	12C5
A1J6-32	-HAR 8	3309780	12C5
A1J6-33	-HAR 1	3309780	12C5
A1J6-34	-HAR 2	3309780	12C5
A1J8-01	-COLUMN X2	3309780	12C4
A1J8-02	-COLUMN X1	3309780	12C4
A1J8-03	-COLUMN X4	3309780	12C4
A1J8-04	-COLUMN X3	3309780	12C4
A1J8-05	-ROW Y4	3309780	12C4
A1J8-06	-ROW Y3	3309780	12C4
A1J8-07	-ROW Y2	3309780	12C4
A1J8-08	-ROW Y1	3309780	12C4
A1J8-09	+D4SD	3309780	12B4
A1J8-10	+D4SE	3309780	12B4
A1J8-11	+D4SC	3309780	12B4
A1J8-12	+D4SB	3309780	12B4
A1J8-13	+D4SA	3309780	12B4
A1J8-14	+D4SG	3309780	12B4
A1J8-15	+D4SF	3309780	12B4
A1J8-16	+D2SB	3309780	12C4
A1J8-17	+D2SC	3309780	12C4
A1J8-18	+D2SD	3309780	12C4
A1J8-19	+D2SE	3309780	12C4
A1J8-20	+D2SA	3309780	12C4
A1J8-21	+D2SG	3309780	12C4
A1J8-22	+D2SF	3309780	12C4
A1J8-23	+D1SF	3309780	12C4
A1J8-24	+D1SG	3309780	12C4
A1J8-25	+D1SA	3309780	12C4
A1J8-26	+D1SB	3309780	12C4

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1J8-27	+D1SC	3309780	12C4
A1J8-28	+D1SD	3309780	12C4
A1J8-29	+D1SE	3309780	12C4
A1J8-31	+D3SG	3309780	12B4
A1J8-32	+D3SA	3309780	12C4
A1J8-33	+D3SB	3309780	12B4
A1J8-34	+D3SC	3309780	12B4
A1J8-35	+D3SD	3309780	12B4
A1J8-36	+D3SE	3309780	12B4
A1J8-37	-DIAGNOSTICS SWITCH (DIAGNOSTIC)	3309780	12C4
A1J8-39	-RD ONLY LED (-READ ONLY LED)	3309780	12A4
A1J8-40	-SELECT LED (-SELECTED LED)	3309780	12A4
A1J8-41	-READY LED	3309780	12B4
A1J8-42	-FAULT RESET SW	3309780	12C4
A1J8-43	-UNSAFE LED (-FAULT LED)	3309780	12A4
A1J8-44	-READ ONLY SW	3309780	12C4
A1J9-06	-RUN	3309780	1D2
A1J9-07	-START	3309780	1D3
A1J9-08	-POWER FAIL (-PWR FAIL)	3309780	1C4
A1K1-07	-BSQ0	3309780	4A2
A1R15-05	-B SELECTED	3309780	4C7
A1R15-07	-DIAGNOSTICS SWITCH (DIAGNOSTIC)	3309780	4C8
A1RP-01	ABS5-P	3309780	2B7
A1RP-02	-B BUS 0	3309780	2D6
A1RP-02	-D BUS 0	3309780	2D6
A1RP-02*	-BUS 0	3309780	2D5
A1RP-03	-D BUS 2	3309780	2C6
A1RP-03	-B BUS 2	3309780	2C6
A1RP-03*	-BUS 2	3309780	2C5
A1RP-04	-D BUS 3	3309780	2C6
A1RP-04	-B BUS 3	3309780	2C6
A1RP-04*	-BUS 3	3309780	2C5
A1RP-05	-D BUS 5	3309780	2B6
A1RP-05	-B BUS 5	3309780	2B6
A1RP-05*	-BUS 5	3309780	2B4
A1RP-06	-B BUS 4	3309780	2B6
A1RP-06*	-BUS 4	3309780	2B4
A1RP-07	-B BUS 6	3309780	2B6
A1RP-07*	-BUS 6	3309780	2B6
A1RP-08	-D BUS 1	3309780	2D6
A1RP-08	-B RESERVED	3309780	4B7
A1RP-08	-B BUS 1	3309780	2D6
A1RP-08	-B BUS 7	3309780	2A6
A1RP-08*	-BUS 7	3309780	2A6
A1RP-08*	-BUS 1	3309780	2D5
A1RP1-03	-A CONTROL TAG	3309780	2B2
A1RP1-03	-A CONTROL TAG	3309780	2B1
A1RP1-04	-B BUS 10	3309780	2D2
A1RP1-04*	-BUS 10	3309780	2D2
A1RP1-05	-BUS 8	3309780	2D2
A1RP1-06	-CYLINDER TAG	3309780	2C2
A1RP1-07	-HEAD TAG (-HD TAG)	3309780	2C2
A1RP10-01	ABS6-P	3309780	2B7
A1RP10-04	ABS6-N	3309780	2B7
A1RP10-05	ABS7-P	3309780	2B7

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1RP10-07	ABS7-N	3309780	2B7
A1RP13-02	AWDT-P	3309780	2B4
A1RP13-04	AWDT-N	3309780	2B4
A1RP13-06	AWCK-N	3309780	2A4
A1RP13-19	AWCK-P	3309780	2A4
A1RP15-03	-A INHIBIT	3309780	4B7
A1RP15-04	-BHL 1	3309780	4B7
A1RP15-06	+A RESERVED	3309780	4C7
A1RP15-09	-B BUS 9	3309780	4B7
A1RP21-02	-SELECT SW0	3309780	4C7
A1RP21-03	-SELECT SW1	3309780	4C7
A1RP21-04	-SELECT SW2	3309780	4C7
A1RP21-05	-SELECT SW3	3309780	4C7
A1RP5-02	ABS8-P	3309780	2D3
A1RP5-04	ABS8-N	3309780	2D3
A1RP5-05	AB10-N	3309780	2D3
A1RP5-07	AB10-P	3309780	2D3
A1RP6-01	AFT1-P	3309780	2C3
A1RP6-04	AFT1-N	3309780	2C3
A1RP6-05	AFT2-P	3309780	2C3
A1RP6-07	AFT2-N	3309780	2C3
A1RP7-01	ABS1-P	3309780	2D7
A1RP7-04	ABS1-N	3309780	2D7
A1RP7-05	ABS0-N	3309780	2D7
A1RP7-07	ABS0-P	3309780	2D7
A1RP8-01	ABS2-P	3309780	2D7
A1RP8-04	ABS2-N	3309780	2D7
A1RP8-05	ABS3-P	3309780	2D7
A1RP8-07	ABS3-N	3309780	2D7
A1RP9-04	ABS5-N	3309780	2B7
A1RP9-05	ABS4-N	3309780	2B7
A1RP9-07	ABS4-P	3309780	2B7
A1S4-01*	-SELECT SW0	3309780	4C7
A1S4-02*	-SELECT SW1	3309780	4C7
A1S4-03*	-SELECT SW2	3309780	4C7
A1S4-04*	-SELECT SW3	3309780	4C7
A1U10-01	-SELECT SW3	3309780	4C6
A1U10-03	-OPEN CABLE DETECT	3309780	4C6
A1U10-09	-SELECT SW0	3309780	4C6
A1U10-11	-SELECT SW1	3309780	4C6
A1U10-12	I/O BUS B1	3309780	11A7
A1U10-13	-RESET	3309780	11A7
A1U10-14	-SELECT SW2	3309780	4C6
A1U100-03	+INDEX	3309780	11A7
A1U100-05*	+INDEX FOUND	3309780	11A6
A1U100-06*	-D CONTROL TAG	3309780	11A6
A1U100-07*	+READ	3309780	11A4
A1U101-01	-RESET	3309780	11A7
A1U101-02	I/O BUS B0	3309780	11A7
A1U101-03	-OP44	3309780	11A7
A1U104-09	+INDEX	3309780	9B5
A1U105-01	+WRITE	3309780	11B4
A1U106-02	I/O BUS B5	3309780	11B4
A1U106-03	-OP44	3309780	11B4
A1U106-05*	+AM ACTIVE	3309780	11B3

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U106-11	-SERVO SQUARE BITS (SQUARED SERVO BITS)	3309780	8B6
A1U107-11	+9.67 CLOCK	3309780	11B3
A1U108-02	+READ	3309780	11A4
A1U108-05*	+SYNC FOUND	3309780	11A4
A1U108-09*	+WRITE PATTERN	3309780	11B4
A1U108-12	+WRITE	3309780	11B4
A1U109-02	+9.67 CLOCK	3309780	11B7
A1U109-05	+SYNC FOUND	3309780	11C6
A1U109-09	+WRITE PATTERN	3309780	11C6
A1U109-10	+9.67 CLOCK	3309780	1C6
A1U109-12	+SYNC FOUND	3309780	11C4
A1U11-03*	-WRITE DATA	3309780	2B2
A1U11-04	-A PORT ENABLE	3309780	2A3
A1U11-05*	-WRITE CLOCK	3309780	2A2
A1U11-13*	-A CONTROL TAG	3309780	2B2
A1U11-14	AFT3-N	3309780	2B3
A1U11-15	AFT3-P	3309780	2B3
A1U110-01	+WRITE	3309780	11B7
A1U110-02	+AM ACTIVE	3309780	11B7
A1U110-13	+READ	3309780	11B7
A1U111-02	-AM DETECTED	3309780	11C4
A1U111-05	+INDEX FOUND	3309780	11B7
A1U112-02	+UNSAFE	3309780	10C3
A1U112-03*	+UNSAFE CLOCK	3309780	10C1
A1U112-11*	-RESET	3309780	11B5
A1U112-13	-POWER ON RESET	3309780	11B5
A1U113-03,04,07,08	I/O BUS	3309780	11B6
A1U113-11	OP43	3309780	11B6
A1U113-13,14,17,18	I/O BUS	3309780	11B6
A1U114-01	+A OR B SELECTED	3309780	10B2
A1U114-02*	-SELECT LED (-SELECTED LED)	3309780	10B1
A1U114-03	+UNSAFE	3309780	10C2
A1U114-04*	-UNSAFE LED (-FAULT LED)	3309780	10C1
A1U114-06*	-READY LED	3309780	10C1
A1U114-10*	POWER ON RESET	3309780	6A6
A1U114-12*	-RD ONLY LED (-READ ONLY LED)	3309780	10B1
A1U119-01	-IP16	3309780	7C6
A1U119-02*	I/O BUS	3309780	7C5
A1U119-03	+KEY 1	3309780	7C6
A1U119-04	+KEY 2	3309780	7C6
A1U119-05*	I/O BUS	3309780	7C5
A1U119-06*	I/O BUS	3309780	7C5
A1U119-07	+KEY 4	3309780	7B6
A1U119-08	+KEY 8	3309780	7B6
A1U119-09*	I/O BUS	3309780	7C5
A1U119-11	+4 MHZ CLOCK	3309780	7B6
A1U119-12*	I/O BUS	3309780	7C5
A1U119-15*	I/O BUS	3309780	7C5
A1U119-16*	I/O BUS	3309780	7C5
A1U119-19*	I/O BUS	3309780	7C5
A1U12-01	+INDEX	3309780	3B3
A1U12-02*	AIDX-P	3309780	3A2
A1U12-03*	AIDX-N	3309780	3B2
A1U12-04*	ASCT-N	3309780	3A2
A1U12-05*	ASCT-P	3309780	3A2

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U12-06	-DISABLE A	3309780	3A3
A1U12-07	+SECTOR PULSE	3309780	3B3
A1U12-10	+A SELECTED	3309780	3B3
A1U12-11*	ASEL-P	3309780	3B2
A1U12-12*	ASEL-N	3309780	3B2
A1U12-13*	ASKN-N	3309780	3B2
A1U12-14*	ASKN-P	3309780	3B2
A1U12-15	+A SEEK END	3309780	3B3
A1U120-01	-ROW Y1	3309780	10B7
A1U120-02	-ROW Y2	3309780	10A7
A1U120-03	-ROW Y3	3309780	10A7
A1U120-04	-ROW Y4	3309780	10A7
A1U120-07	-COLUMN X4	3309780	10A6
A1U120-08	-COLUMN X3	3309780	10A6
A1U120-10	-COLUMN X2	3309780	10A6
A1U120-11	-COLUMN X1	3309780	10A6
A1U120-12*	+DATA AVAILABLE	3309780	10B6
A1U120-14*	+KEY 8	3309780	10B6
A1U120-15*	+KEY 4	3309780	10B6
A1U120-16*	+KEY 2	3309780	10B6
A1U120-17*	+KEY 1	3309780	10B6
A1U121-03	-OP26	3309780	10A5
A1U121-07,01,02,06	I/O BUS	3309780	10A5
A1U121-09*	+D4SE	3309780	10A5
A1U121-10*	+D4SD	3309780	10A5
A1U121-11*	+D4SC	3309780	10A5
A1U121-12*	+D4SB	3309780	10A5
A1U121-13*	+D4SA	3309780	10A5
A1U121-14*	+D4SG	3309780	10A5
A1U121-15*	+D4SF	3309780	10A5
A1U122-03*	-OP25	3309780	10A3
A1U122-07,01,02,06	I/O BUS	3309780	10A3
A1U122-09*	+D2SE	3309780	10A3
A1U122-10*	+D2SD	3309780	10A3
A1U122-11*	+D2SC	3309780	10A3
A1U122-12*	+D2SB	3309780	10A3
A1U122-13*	+D2SA	3309780	10A3
A1U122-14*	+D2SG	3309780	10A3
A1U122-15*	+D2SF	3309780	10A3
A1U123-03*	-OP25	3309780	10A3
A1U123-07,01,02,06	I/O BUS	3309780	10A2
A1U123-09*	+D1SE	3309780	10A2
A1U123-10*	+D1SD	3309780	10A2
A1U123-11*	+D1SC	3309780	10A2
A1U123-12*	+D1SB	3309780	10A2
A1U123-13*	+D1SA	3309780	10A2
A1U123-14*	+D1SG	3309780	10A2
A1U123-15*	+D1SF	3309780	10A2
A1U124-03	-OP26	3309780	10A4
A1U124-07,01,02,06	I/O BUS	3309780	10A4
A1U124-09*	+D3SE	3309780	10A4
A1U124-10*	+D3SD	3309780	10A4
A1U124-11*	+D3SC	3309780	10A4
A1U124-12*	+D3SB	3309780	10A4
A1U124-13*	+D3SA	3309780	10A4

**ASSY/
COMPONENT/PIN**

TERM

**SCHEM.
DIAGRAM**

**SHEET
COORD.**

A1U124-14*	+D3SG	3309780	10A4
A1U124-15*	+D3SF	3309780	10A4
A1U13-01	-BUS 3	3309780	5B7
A1U13-02*	+BUS 3	3309780	5B7
A1U13-03	-HEAD TAG (-HD TAG)	3309780	5D7
A1U13-05	-BUS 4	3309780	5B7
A1U13-06*	+BUS 4	3309780	5B7
A1U13-08*	+BUS 7	3309780	5B7
A1U13-09	-BUS 7	3309780	5B7
A1U13-10*	BUS 6	3309780	5C5
A1U13-11	-BUS 6	3309780	5C5
A1U14-01	-BUS 2	3309780	5B7
A1U14-02*	+BUS 2	3309780	5B7
A1U14-03	-BUS 1	3309780	5C7
A1U14-04*	+BUS 1	3309780	5C7
A1U14-05	+BUS 10	3309780	7C7
A1U14-08*	+BUS 5	3309780	5B7
A1U14-09	-BUS 5	3309780	5B7
A1U14-10*	+BUS 8	3309780	5A7
A1U14-11	-BUS 8	3309780	5A7
A1U14-12*	+BUS 0	3309780	5C7
A1U14-13	-BUS 0	3309780	5C7
A1U15-01	-A SELECTED	3309780	4C3
A1U15-02	-B SELECTED	3309780	4C3
A1U15-03*	+A OR B SELECTED	3309780	4C3
A1U15-04	+A RESERVED	3309780	4B5
A1U15-06*	-A RELEASE	3309780	4B4
A1U15-08	-B RELEASE	3309780	4B4
A1U15-11*	+BUS 9	3309780	4B4
A1U15-12	-B RELEASE	3309780	4B4
A1U15-13	-A RELEASE	3309780	4B4
A1U16-01	+SEEK INCOMPLETE	3309780	10C3
A1U16-03	+4 MHZ CLOCK	3309780	4C4
A1U16-04*	-4 MHZ CLOCK	3309780	4C4
A1U16-05	-B RESERVED	3309780	4B6
A1U16-06	+B RESERVED	3309780	4B6
A1U16-09	-B BUS 9	3309780	4B5
A1U16-11	-BUS 9	3309780	4B5
A1U16-11	-A BUS 9	3309780	4B5
A1U16-13	-DISABLE A	3309780	1A7
A1U17-01	+READY	3309780	10D2
A1U17-02	-UNSAFE	3309780	10D2
A1U17-03*	+FILE READY	3309780	10D1
A1U17-05	-4 MHZ CLOCK	3309780	4B5
A1U17-08*	-DIAGNOSTICS	3309780	4C6
A1U17-09	-DIAGNOSTICS TEST	3309780	4C7
A1U17-10	-DIAGNOSTICS SWITCH (DIAGNOSTIC)	3309780	4C8
A1U17-11*	-DISABLE A	3309780	4B6
A1U17-12	-A INHIBIT	3309780	4B6
A1U17-13	-DIAGNOSTICS	3309780	4B6
A1U18-01	-DIAGNOSTICS	3309780	4C3
A1U18-02	+A SELECTED	3309780	4D3
A1U18-03	-A CONTROL TAG	3309780	5C8
A1U18-04	-B CONTROL TAG	3309780	5C8
A1U18-05	-D CONTROL TAG	3309780	5C8

ASSY/ COMPONENT/PIN	TRIM	SCHEM. DIAGRAM	SHEET COORD.
A1U18-09	-UNSAFE	3309780	10C2
A1U18-10	+ON CYLINDER	3309780	10C3
A1U18-12*	+A PORT ENABLE	3309780	4D3
A1U18-13	+A RESERVED	3309780	4C3
A1U19-01*	I/O BUS	3309780	7C3
A1U19-02*	-DIFF 2 (-2)	3309780	7B2
A1U19-03*	-DIFF 1 (-1)	3309780	7C2
A1U19-06*	-DIFF 4 (-4)	3309780	7B2
A1U19-07*	-DIFF 8 (-8)	3309780	7B2
A1U19-09*	I/O BUS	3309780	7C3
A1U19-10*	I/O BUS	3309780	7C3
A1U19-11	-OP23	3309780	7B3
A1U19-15*	I/O BUS	3309780	7C3
A1U2-01	ARS3-P	3309780	1C6
A1U2-02	ARS3-N	3309780	1C6
A1U2-03*	-A SELECT 3	3309780	1C5
A1U2-05*	-A SELECT 2	3309780	1C5
A1U2-06	ARS2-N	3309780	1C6
A1U2-07	ARS2-P	3309780	1C6
A1U2-09	ARS0-P	3309780	1D6
A1U2-10	ARS0-N	3309780	1D6
A1U2-11*	-A SELECT 0	3309780	1D5
A1U2-13*	-A SELECT 1	3309780	1C5
A1U2-14	ARS1-N	3309780	1D6
A1U2-15	ARS1-P	3309780	1C6
A1U20-01	+B RESERVED	3309780	3D3
A1U20-08*	ASCK-N	3309780	3C2
A1U20-09*	ASCK-P	3309780	3C2
A1U20-10	-DISABLE A	3309780	3D3
A1U20-12*	TABY-N	3309780	3D2
A1U20-13*	TABY-P	3309780	3D2
A1U21-01	-READ CLOCK BUF 2 (-CLOCK)	3309780	3B3
A1U21-03	+A SELECTED	3309780	3D3
A1U21-06	-READ DATA BUF 2 (-DATA)	3309780	3C3
A1U21-08*	ARDT-N	3309780	3C3
A1U21-09*	ARDT-P	3309780	3C2
A1U21-10	-DISABLE A	3309780	3A10
A1U21-12*	ARCK-P	3309780	3C2
A1U21-13*	ARCK-N	3309780	3C2
A1U22-03*	-D BUS 0	3309780	11A5
A1U22-06*	-HEAD TAG (-HD TAG)	3309780	11C2
A1U22-08*	-WRITE CLOCK	3309780	11A6
A1U22-10	+9.67 CLOCK	3309780	11A7
A1U22-11*	-WRITE DATA	3309780	11C2
A1U22-13	+WRITE	3309780	11C2
A1U23-03	+EN SEQ TNU	3309780	4A3
A1U23-08*	-D BUS 5	3309780	11B2
A1U23-12*	-D BUS 1	3309780	11A5
A1U24-01	+DHAR2	3309780	11D2
A1U24-03*	-D BUS 1	3309780	11D2
A1U24-04	+DHAR4	3309780	11D2
A1U24-06*	-D BUS 2	3309780	11D2
A1U24-08*	-D BUS 3	3309780	11D2
A1U24-09	+DHAR8	3309780	11D2
A1U24-11*	-D BUS 0	3309780	11D2

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U124-14*	+D3SG	3309780	10A4
A1U124-15*	+D3SF	3309780	10A4
A1U13-01	-BUS 3	3309780	5B7
A1U13-02*	+BUS 3	3309780	5B7
A1U13-03	-HEAD TAG (-HD TAG)	3309780	5D7
A1U13-05	-BUS 4	3309780	5B7
A1U13-06*	+BUS 4	3309780	5B7
A1U13-08*	+BUS 7	3309780	5B7
A1U13-09	-BUS 7	3309780	5B7
A1U13-10*	BUS 6	3309780	5C5
A1U13-11	-BUS 6	3309780	5C5
A1U14-01	-BUS 2	3309780	5B7
A1U14-02*	+BUS 2	3309780	5B7
A1U14-03	-BUS 1	3309780	5C7
A1U14-04*	+BUS 1	3309780	5C7
A1U14-05	+BUS 10	3309780	7C7
A1U14-08*	+BUS 5	3309780	5B7
A1U14-09	-BUS 5	3309780	5B7
A1U14-10*	+BUS 8	3309780	5A7
A1U14-11	-BUS 8	3309780	5A7
A1U14-12*	+BUS 0	3309780	5C7
A1U14-13	-BUS 0	3309780	5C7
A1U15-01	-A SELECTED	3309780	4C3
A1U15-02	-B SELECTED	3309780	4C3
A1U15-03*	+A OR B SELECTED	3309780	4C3
A1U15-04	+A RESERVED	3309780	4B5
A1U15-06*	-A RELEASE	3309780	4B4
A1U15-08	-B RELEASE	3309780	4B4
A1U15-11*	+BUS 9	3309780	4B4
A1U15-12	-B RELEASE	3309780	4B4
A1U15-13	-A RELEASE	3309780	4B4
A1U16-01	+SEEK INCOMPLETE	3309780	10C3
A1U16-03	+4 MHZ CLOCK	3309780	4C4
A1U16-04*	-4 MHZ CLOCK	3309780	4C4
A1U16-05	-B RESERVED	3309780	4B6
A1U16-06	+B RESERVED	3309780	4B6
A1U16-09	-B BUS 9	3309780	4B5
A1U16-11	-BUS 9	3309780	4B5
A1U16-11	-A BUS 9	3309780	4B5
A1U16-13	-DISABLE A	3309780	1A7
A1U17-01	+READY	3309780	10D2
A1U17-02	-UNSAFE	3309780	10D2
A1U17-03*	+FILE READY	3309780	10D1
A1U17-05	-4 MHZ CLOCK	3309780	4B5
A1U17-08*	-DIAGNOSTICS	3309780	4C6
A1U17-09	-DIAGNOSTICS TEST	3309780	4C7
A1U17-10	-DIAGNOSTICS SWITCH (DIAGNOSTIC)	3309780	4C8
A1U17-11*	-DISABLE A	3309780	4B6
A1U17-12	-A INHIBIT	3309780	4B6
A1U17-13	-DIAGNOSTICS	3309780	4B6
A1U18-01	-DIAGNOSTICS	3309780	4C3
A1U18-02	+A SELECTED	3309780	4D3
A1U18-03	-A CONTROL TAG	3309780	5C8
A1U18-04	-B CONTROL TAG	3309780	5C8
A1U18-05	-D CONTROL TAG	3309780	5C8

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U18-09	-UNSAFE	3309780	10C2
A1U18-10	+ON CYLINDER	3309780	10C3
A1U18-12*	+A PORT ENABLE	3309780	4D3
A1U18-13	+A RESERVED	3309780	4C3
A1U19-01*	I/O BUS	3309780	7C3
A1U19-02*	-DIFF 2 (-2)	3309780	7B2
A1U19-03*	-DIFF 1 (-1)	3309780	7C2
A1U19-06*	-DIFF 4 (-4)	3309780	7B2
A1U19-07*	-DIFF 8 (-8)	3309780	7B2
A1U19-09*	I/O BUS	3309780	7C3
A1U19-10*	I/O BUS	3309780	7C3
A1U19-11	-OP23	3309780	7B3
A1U19-15*	I/O BUS	3309780	7C3
A1U2-01	ARS3-P	3309780	1C6
A1U2-02	ARS3-N	3309780	1C6
A1U2-03*	-A SELECT 3	3309780	1C5
A1U2-05*	-A SELECT 2	3309780	1C5
A1U2-06	ARS2-N	3309780	1C6
A1U2-07	ARS2-P	3309780	1C6
A1U2-09	ARS0-P	3309780	1D6
A1U2-10	ARS0-N	3309780	1D6
A1U2-11*	-A SELECT 0	3309780	1D5
A1U2-13*	-A SELECT 1	3309780	1C5
A1U2-14	ARS1-N	3309780	1D6
A1U2-15	ARS1-P	3309780	1C6
A1U20-01	+B RESERVED	3309780	3D3
A1U20-08*	ASCK-N	3309780	3C2
A1U20-09*	ASCK-P	3309780	3C2
A1U20-10	-DISABLE A	3309780	3D3
A1U20-12*	TABY-N	3309780	3D2
A1U20-13*	TABY-P	3309780	3D2
A1U21-01	-READ CLOCK BUF 2 (-CLOCK)	3309780	3B3
A1U21-03	+A SELECTED	3309780	3D3
A1U21-06	-READ DATA BUF 2 (-DATA)	3309780	3C3
A1U21-08*	ARDT-N	3309780	3C3
A1U21-09*	ARDT-P	3309780	3C2
A1U21-10	-DISABLE A	3309780	3A10
A1U21-12*	ARCK-P	3309780	3C2
A1U21-13*	ARCK-N	3309780	3C2
A1U22-03*	-D BUS 0	3309780	11A5
A1U22-06*	-HEAD TAG (-HD TAG)	3309780	11C2
A1U22-08*	-WRITE CLOCK	3309780	11A6
A1U22-10	+9.67 CLOCK	3309780	11A7
A1U22-11*	-WRITE DATA	3309780	11C2
A1U22-13	+WRITE	3309780	11C2
A1U23-03	+EN SEQ TNU	3309780	4A3
A1U23-08*	-D BUS 5	3309780	11B2
A1U23-12*	-D BUS 1	3309780	11A5
A1U24-01	+DHAR2	3309780	11D2
A1U24-03*	-D BUS 1	3309780	11D2
A1U24-04	+DHAR4	3309780	11D2
A1U24-06*	-D BUS 2	3309780	11D2
A1U24-08*	-D BUS 3	3309780	11D2
A1U24-09	+DHAR8	3309780	11D2
A1U24-11*	-D BUS 0	3309780	11D2

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U24-12	+DHAR1	3309780	11D2
A1U25-01	+A SEEK END	3309780	4B3
A1U25-06	+ON CYLINDER	3309780	4A3
A1U25-10*	-DIFF CLOCK	3309780	8B3
A1U26-06*	-A RAW SELECT	3309780	4C5
A1U26-08*	-A SELECTED	3309780	4C3
A1U26-09*	+A SELECTED	3309780	4C3
A1U26-11	-4 MHZ CLOCK	3309780	4D4
A1U27-01	-SERVO CLOCK (+SERVO CLOCK TTL)	3309780	8C7
A1U27-03	-9.67 CLOCK BUF 1	3309780	8C7
A1U29-02*, A1U29-14	-SEQUENCE PICK	3309780	4A6
A1U29-07	-AHL 1	3309780	4B6
A1U29-12*, A1U29-07	-SEQUENCE HOLD	3309780	4B6
A1U3-03*	-CYLINDER TAG	3309780	2C2
A1U3-05*	-HEAD TAG (-HD TAG)	3309780	2C2
A1U3-06*	-DIFF 64 (-64)	3309780	7C2
A1U30-01*	I/O BUS	3309780	7D3
A1U30-02*	-DIFF 512 (-512)	3309780	7D2
A1U30-03*	-DIFF 256 (-256)	3309780	7D2
A1U30-06*	-DIFF 1024 (-1024)	3309780	7D2
A1U30-09*	I/O BUS	3309780	7D3
A1U30-10*	I/O BUS	3309780	7D3
A1U30-11	-OP24	3309780	7D4
A1U30-12*	->DIFF 256	3309780	7D2
A1U30-15*	I/O BUS	3309780	7D3
A1U31-01*	I/O BUS	3309780	7C3
A1U31-02*	-DIFF 32 (-32)	3309780	7C2
A1U31-03*	-DIFF 16 (-16)	3309780	7C2
A1U31-07*	-DIFF 128 (-128)	3309780	7C2
A1U31-09*	I/O BUS	3309780	7C3
A1U31-10*	I/O BUS	3309780	7C3
A1U31-11	-OP24	3309780	7C3
A1U31-15*	I/O BUS	3309780	7C3
A1U32-05	-CYL PULSE	3309780	8A3
A1U32-12	-CYL PULSE	3309780	8B3
A1U33-01	+BUS 8	3309780	5A6
A1U33-03*	-STROBE LATE	3309780	5A6
A1U33-04	+BUS 4	3309780	5B6
A1U33-06	-CONTROLLER RESET	3309780	5B6
A1U33-08*	-STROBE EARLY	3309780	5B6
A1U33-09	+BUS 7	3309780	5B6
A1U33-11*	-ADDRESS MARK ENABLE (-AM ENABLE)	3309780	5B6
A1U33-12	+BUS 5	3309780	5B6
A1U34-01*	-OFFSET SELECT	3309780	5B5
A1U34-02	+OFFSET REVERSE	3309780	5B6
A1U34-03	+OFFSET FORWARD	3309780	5B6
A1U35-02*	+4 MHZ CLOCK	3309780	6C7
A1U35-03	-A SELECT ENABLE	3309780	4C6
A1U35-08*	-UNSAFE	3309780	10D3
A1U35-09	+UNSAFE	3309780	10D3
A1U35-11	-OP45	3309780	11D3
A1U35-12*	-A SELECT ENABLE	3309780	1B5
A1U36-01	-INTERRUPT	3309780	5B3
A1U36-02	+ON TRACK	3309780	5B3
A1U36-03*	+ON CYLINDER	3309780	5B3

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U36-05	-POWER ON RESET	3309780	4C5
A1U36-08*	+OFFSET FORWARD	3309780	5B6
A1U36-09	+BUS 2	3309780	5D6
A1U36-11*	+OFFSET REVERSE	3309780	5B6
A1U36-13	+BUS 3	3309780	5B6
A1U37-03*	-A PORT ENABLE	3309780	4D3
A1U37-04	+BUS 0	3309780	5C6
A1U37-06*	-WRITE GATE	3309780	5C6
A1U37-08*	-READ GATE	3309780	5C6
A1U37-09	+BUS 1	3309780	5D6
A1U37-13	-A SELECT ENABLE	3309780	4D6
A1U38-02	+SEEK INCOMPLETE	3309780	5B4
A1U38-03	+OFFSET REVERSE	3309780	5B4
A1U38-04	-RESET INTERRUPT	3309780	5B4
A1U38-10	-RESET INTERRUPT	3309780	5B4
A1U38-11	+OFFSET FORWARD	3309780	5B4
A1U38-12	+SEEK INCOMPLETE	3309780	5C4
A1U39-04	-RESET INTERRUPT	3309780	5C4
A1U39-06*	+REZERO INT	3309780	5C4
A1U39-08*	+SEEK INT	3309780	5A4
A1U39-10	-RESET INTERRUPT	3309780	5A4
A1U39-11	-CYLINDER TAG	3309780	5A4
A1U39-12	+SEEK INCOMPLETE	3309780	5A4
A1U4-04	-A PORT ENABLE	3309780	2A7
A1U40-02	-9.67 CLOCK BUF 1	3309780	3D5
A1U40-03*	-9.67 CLOCK BUF 1	3309780	3D5
A1U40-04	-WRITE DATA	3309780	3C5
A1U40-05*	-WRITE CLOCK BUF (-WRITE CLK)	3309780	3C4
A1U40-06	-READ DATA	3309780	3B5
A1U40-07*	-READ DATA BUF 2 (-DATA)	3309780	3C4
A1U40-08	-READ CLOCK	3309780	3B5
A1U40-09*	-READ CLOCK BUF 2 (-CLOCK)	3309780	3B4
A1U40-11	-READ CLOCK BUF 1	3309780	3B5
A1U40-12*	-READ CLOCK BUF 1	3309780	3B4
A1U40-13	-READ DATA BUF 1	3309780	3C5
A1U40-14*	-READ DATA BUF 1	3309780	3B4
A1U40-15	-WRITE CLOCK	3309780	3C5
A1U40-16*	-WRITE DATA BUF	3309780	3C4
A1U40-17	-PLO (9.67 MHZ)	3309780	3D5
A1U40-18*	-9.67 CLOCK BUF 2 (-9.67 CLK)	3309780	3D4
A1U41-01	-POWER ON RESET	3309780	7C4
A1U41-03*	I/O BUS	3309780	7D4
A1U41-04*	I/O BUS	3309780	7D4
A1U41-05*	-MOVE OUT	3309780	7D4
A1U41-06*	-OFFSET	3309780	7D4
A1U41-07*	I/O BUS	3309780	7D4
A1U41-08*	I/O BUS	3309780	7D4
A1U41-09*	-LOCK ON	3309780	7D4
A1U41-11	-OP20	3309780	7D4
A1U41-12*	+ON TRACK	3309780	7D4
A1U41-13*	I/O BUS	3309780	7D4
A1U41-14*	I/O BUS	3309780	7D4
A1U41-15*	+READY	3309780	7C4
A1U41-16*	-SERVO DISABLE	3309780	7C4
A1U41-17*	I/O BUS	3309780	7D4

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U41-18*	I/O BUS	3309780	7D4
A1U41-19*	+SEEK INCOMPLETE	3309780	7C4
A1U42-01	-POWER ON RESET	3309780	7C4
A1U42-02*	+CAR 1	3309780	7C4
A1U42-03*	I/O BUS	3309780	7C4
A1U42-04*	I/O BUS	3309780	7C4
A1U42-05*	+CAR 2	3309780	7C4
A1U42-06*	+ODD HEAD	3309780	7C4
A1U42-07*	I/O BUS	3309780	7C4
A1U42-08*	I/O BUS	3309780	7C4
A1U42-09*	+SPLIT FIELD	3309780	7C4
A1U42-11	-OP21	3309780	7C4
A1U42-12*	-OUTER TRACK	3309780	7C4
A1U42-13*	I/O BUS	3309780	7C4
A1U42-14*	I/O BUS	3309780	7C4
A1U42-15*	+EN SEQ TNU	3309780	7C4
A1U42-17*	I/O BUS	3309780	7C4
A1U42-18*	I/O BUS	3309780	7C4
A1U42-19*	+RUN	3309780	7C4
A1U43-01	-POWER ON RESET	3309780	7B4
A1U43-02*	-DIAGNOSTICS TEST	3309780	7B3
A1U43-03*	I/O BUS	3309780	7C4
A1U43-04*	I/O BUS	3309780	7C4
A1U43-07*	I/O BUS	3309780	7C4
A1U43-08*	I/O BUS	3309780	7C4
A1U43-11	-OP22	3309780	7C4
A1U43-13*	I/O BUS	3309780	7C4
A1U43-14*	I/O BUS	3309780	7C4
A1U43-17*	I/O BUS	3309780	7C4
A1U43-18*	I/O BUS	3309780	7C4
A1U44-02*	I/O BUS	3309780	7C7
A1U44-03	+BUS 8	3309780	7C7
A1U44-04	+BUS 9	3309780	7C7
A1U44-05*	I/O BUS	3309780	7C7
A1U44-06*	I/O BUS	3309780	7C7
A1U44-09*	I/O BUS	3309780	7C7
A1U44-11	+CYLINDER TAG	3309780	7C7
A1U44-12*	I/O BUS	3309780	7C7
A1U44-15*	I/O BUS	3309780	7C7
A1U44-16*	I/O BUS	3309780	7C7
A1U44-19*	I/O BUS	3309780	7C7
A1U45-01	-IP10	3309780	7D7
A1U45-02*	I/O BUS	3309780	7D7
A1U45-03	+BUS 0	3309780	7D7
A1U45-04	+BUS 1	3309780	7D7
A1U45-05*	I/O BUS	3309780	7D7
A1U45-06*	I/O BUS	3309780	7D7
A1U45-07	+BUS 2	3309780	7D7
A1U45-08	+BUS 3	3309780	7D7
A1U45-09*	I/O BUS	3309780	7D7
A1U45-11	+CYLINDER TAG	3309780	7C7
A1U45-12*	I/O BUS	3309780	7D7
A1U45-13	+BUS 4	3309780	7D7
A1U45-14	+BUS 5	3309780	7D7
A1U45-15*	I/O BUS	3309780	7D7

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U45-16*	I/O BUS	3309780	7D7
A1U45-17	+BUS 6	3309780	7C7
A1U45-18	+BUS 7	3309780	7C7
A1U45-19*	I/O BUS	3309780	7D7
A1U46-02*	+DHAR 1	3309780	11D7
A1U46-03,04,07,08	I/O BUS	3309780	11D7
A1U46-05*	+DHAR 2	3309780	11D7
A1U46-06*	+DHAR 4	3309780	11D7
A1U46-09*	+DHAR 8	3309780	11D7
A1U46-11	-OP40	3309780	11D7
A1U46-13,14,17,18	I/O BUS	3309780	11D7
A1U50-03,04,07,08	I/O BUS	3309780	11D5
A1U50-11	-OP42	3309780	11D5
A1U51-08*	-INTERRUPT	3309780	5B3
A1U52-01	+SERVO ONE BYTE (+SERVO ONE BYTE TTL)	3309780	8D7
A1U52-06*	-INDEX RESET	3309780	8C7
A1U52-08	-SERVO CLOCK (+SERVO CLOCK TTL)	3309780	8D7
A1U52-09	+RUN	3309780	8D7
A1U53-10*	-INDEX ENABLE	3309780	8C6
A1U55-01	-INITIALIZE	3309780	5C6
A1U55-04	+BUS 3	3309780	5D6
A1U55-06	+BUS 2	3309780	5D6
A1U55-11	+BUS 1	3309780	5D6
A1U55-13	+BUS 0	3309780	5D6
A1U56-03,04,07,08	I/O BUS	3309780	11D6
A1U56-11	-OP41	3309780	11D6
A1U56-13,14,17,18	I/O BUS	3309780	11D6
A1U59-09	-DIAGNOSTICS	3309780	11B5
A1U59-10*	-REZERO	3309780	7C3
A1U59-12*	-OPEN CABLE DETECT	3309780	1B5
A1U6-01	ARSL-P	3309780	1B6
A1U6-02	ARSL-N	3309780	1B6
A1U6-09	ABS9-P	3309780	1A6
A1U6-10	ABS9-N	3309780	1A6
A1U6-11*	-A BUS 9	3309780	1A5
A1U6-14	ARDV-N	3309780	1B6
A1U6-15	ARDV-P	3309780	1B6
A1U60-06*	OGB #2	3309780	8B3
A1U60-10*	+OGB #1	3309780	8C3
A1U63-01	+SPLIT FIELD	3309780	5C5
A1U63-03	+ODD HEAD	3309780	5C6
A1U63-04*	-HAR 1	3309780	5C5
A1U63-07*	-HAR 2	3309780	5C5
A1U63-09*	-HAR 4	3309780	5C5
A1U63-12*	-HAR 8	3309780	5C5
A1U64-01	-IP15	3309780	7C6
A1U64-02*	I/O BUS	3309780	7C5
A1U64-03	-MODULE 1	3309780	7C6
A1U64-04	-MODULE 2	3309780	7C6
A1U64-05*	I/O BUS	3309780	7C5
A1U64-06*	I/O BUS	3309780	7C5
A1U64-07	-MODULE 4	3309780	7C6
A1U64-08	-MODULE 8	3309780	7C6
A1U64-09*	I/O BUS	3309780	7C5
A1U64-11	+4 MHZ CLOCK	3309780	7C6

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U64-12*	I/O BUS	3309780	7C5
A1U64-13	+SEEK INT	3309780	7C6
A1U64-14	+REZERO INT	3309780	7C6
A1U64-15*	I/O BUS	3309780	7C5
A1U64-16*	I/O BUS	3309780	7C5
A1U64-17	+OFFSET FORWARD	3309780	7C6
A1U64-18	+OFFSET REVERSE	3309780	7C6
A1U64-19*	I/O BUS	3309780	7C5
A1U65-11* THRU 18*	I/O BUS	3309780	6B3
A1U67-16	-INTERRUPT	3309780	6C6
A1U67-17	-POWER FAIL (-PWR FAIL)	3309780	6B6
A1U67-26	POWER ON RESET	3309780	6A6
A1U68-08*	+DIFF <>0	3309780	7C2
A1U68-12	-RESET GB ERROR	3309780	8D4
A1U68-13	-INDEX ENABLE	3309780	8C6
A1U69-08*	-DIFF <>0	3309780	7D2
A1U69-10*	-START	3309780	7C3
A1U69-12*	-RUN	3309780	7C4
A1U7-01	+INDEX	3309780	3C8
A1U7-02*	TAIN-P	3309780	3C7
A1U7-03*	TAIN-N	3309780	3C7
A1U7-04*	TACY-N	3309780	3C7
A1U7-05*	TACY-P	3309780	3C7
A1U7-06	+A PORT ENABLE	3309780	3C8
A1U7-07	+ON CYLINDER	3309780	3D8
A1U7-10	+UNSAFE	3309780	3D8
A1U7-11*	TAFT-P	3309780	3D7
A1U7-12*	TAFT-N	3309780	3D7
A1U7-13*	TASE-N	3309780	3D7
A1U7-14*	TASE-P	3309780	3D7
A1U7-15	+SEEK INCOMPLETE	3309780	3D8
A1U70-09*	-OP26	3309780	6C2
A1U70-10*	-OP25	3309780	6C2
A1U70-11*	-OP24	3309780	6C2
A1U70-12*	-OP23	3309780	6C2
A1U70-13*	-OP22	3309780	6C2
A1U70-14*	-OP21	3309780	6C2
A1U70-15*	-OP20	3309780	6C2
A1U71-11*	-RESET GB ERROR	3309780	6A2
A1U71-12*	-OP43	3309780	6B2
A1U71-13*	-RESET INTERRUPT	3309780	6A2
A1U71-14*	-RESET UNSAFE	3309780	6B2
A1U71-15*	-SET UNSAFE	3309780	6B2
A1U72-07*	-IP17	3309780	6C2
A1U72-09*	-IP16	3309780	6C2
A1U72-10*	-IP15	3309780	6C2
A1U72-11*	-IP14	3309780	6C2
A1U72-12*	-IP13	3309780	6D2
A1U72-13*	-IP12	3309780	6D2
A1U72-14*	-IP11	3309780	6D2
A1U72-15*	-IP10	3309780	6D2
A1U73-10*	-OP45	3309780	6B2
A1U73-11*	-OP44	3309780	6B2
A1U73-12*	-INITIALIZE	3309780	6A2
A1U73-13*	-OP42	3309780	6B2

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U73-14*	-OP41	3309780	6B2
A1U73-15*	-OP40	3309780	6B2
A1U74-03	+PLO UNSAFE (+PLO UNSAFE TTL)	3309780	10D7
A1U74-08*	+9.67 CLOCK	3309780	11C7
A1U74-09	-9.67 CLOCK BUF 1	3309780	11C8
A1U74-11	-READ DATA BUF 1	3309780	11C4
A1U74-13	-READ CLOCK BUF 1	3309780	11C8
A1U75-04	-FINE TRACK	3309780	10C7
A1U76-03	-SET UNSAFE	3309780	10D4
A1U76-04*	+UNSAFE	3309780	10C3
A1U76-09*	+GB ERROR	3309780	8C3
A1U76-10	-RESET GB ERROR	3309780	8C6
A1U77-01	-RESET UNSAFE	3309780	10C4
A1U77-02	-POWER ON RESET	3309780	10C4
A1U77-04	-FAULT RESET SW	3309780	10C4
A1U77-05	-CONTROLLER RESET	3309780	10C4
A1U77-10	-R/W UNSAFE (-GATED R/W UNSAFE)	3309780	10C4
A1U77-12	-MULTI CHIP SEL (-GATED MULT HD)	3309780	10C4
A1U77-13	-POWER FAIL (-PWR FAIL)	3309780	10C4
A1U8-01	+WRITE PROTECT	3309780	3A8
A1U8-02*	TAWP-P	3309780	3A7
A1U8-03*	TAWP-N	3309780	3A7
A1U8-04*	TASC-N	3309780	3B7
A1U8-05*	TASC-P	3309780	3A7
A1U8-06	+A PORT ENABLE	3309780	3A8
A1U8-07	+SECTOR PULSE	3309780	3A8
A1U8-10	+FILE READY	3309780	3C8
A1U8-11*	TARD-P	3309780	3B7
A1U8-12*	TARD-N	3309780	3B7
A1U8-13*	TAMK-P	3309780	3B7
A1U8-14*	TAMK-N	3309780	3B7
A1U8-15	-AM DETECTED	3309780	3B8
A1U82-13*	+INWARD	3309780	10C5
A1U82-14*	+OUTWARD	3309780	10B5
A1U83-02	-MED VEL (-M VEL)	3309780	7A5
A1U83-13	-FINE TRACK	3309780	10C6
A1U84-02	-OFFSET SELECT	3309780	10D6
A1U84-03	-READ ONLY SW	3309780	10D6
A1U84-04	-READ GATE	3309780	10D6
A1U84-05	-WRITE GATE	3309780	10D6
A1U84-06*	-ERROR 4	3309780	10D6
A1U84-07*	-ERROR 2	3309780	10D6
A1U84-09*	-ERROR 1	3309780	10D6
A1U84-14*	-WRITE ERROR	3309780	10C6
A1U85-01	-IP12	3309780	7C7
A1U85-02*	I/O BUS	3309780	7C7
A1U85-03	-ERROR 1	3309780	7C7
A1U85-04	-ERROR 2	3309780	7C7
A1U85-05*	I/O BUS	3309780	7C7
A1U85-06*	I/O BUS	3309780	7C7
A1U85-07	-ERROR 4	3309780	7B7
A1U85-08	-WRITE ERROR	3309780	7B7
A1U85-09*	I/O BUS	3309780	7C7
A1U85-12*	I/O BUS	3309780	7C7
A1U85-13	-MULTI CHIP SEL (-GATED MULT HD)	3309780	7B7

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U85-14	-R/W UNSAFE (-GATED R/W UNSAFE)	3309780	7B7
A1U85-15*	I/O BUS	3309780	7C7
A1U85-16*	I/O BUS	3309780	7C7
A1U85-17	-POWER FAIL (-PWR FAIL)	3309780	7B7
A1U85-19*	I/O BUS	3309780	7C7
A1U86-01	-IP14	3309780	7D6
A1U86-02*	I/O BUS	3309780	7D5
A1U86-03	+OGB #1	3309780	7D6
A1U86-04	+OGB #2	3309780	7D6
A1U86-05*	I/O BUS	3309780	7D5
A1U86-06*	I/O BUS	3309780	7D5
A1U86-07	+DIFF#0	3309780	7D6
A1U86-08	-FINE TRACK	3309780	7D6
A1U86-09*	I/O BUS	3309780	7D5
A1U86-11	+4 MHZ CLOCK	3309780	7D6
A1U86-12*	I/O BUS	3309780	7D5
A1U86-13	+INWARD	3309780	7D6
A1U86-14	+OUTWARD	3309780	7D6
A1U86-15*	I/O BUS	3309780	7D5
A1U86-16*	I/O BUS	3309780	7D5
A1U86-19*	I/O BUS	3309780	7D5
A1U87-01	-IP13	3309780	7B7
A1U87-02*	I/O BUS	3309780	7B7
A1U87-03	-SEQUENCE PICK	3309780	7B7
A1U87-04	-SEQUENCE HOLD	3309780	7B7
A1U87-05*	I/O BUS	3309780	7B7
A1U87-06*	I/O BUS	3309780	7B7
A1U87-07	+UPSPEED	3309780	7B7
A1U87-08	+UNSAFE	3309780	7B7
A1U87-09*	I/O BUS	3309780	7B7
A1U87-11	+4 MHZ CLOCK	3309780	7A7
A1U87-12*	I/O BUS	3309780	7B7
A1U87-13	-POWER FAIL (-PWR FAIL)	3309780	7B7
A1U87-14	+GB ERROR	3309780	7B7
A1U87-15*	I/O BUS	3309780	7B7
A1U87-16*	I/O BUS	3309780	7B7
A1U87-17	+DATA AVAILABLE	3309780	7B7
A1U87-18	-DIAGNOSTICS	3309780	7B7
A1U87-19*	I/O BUS	3309780	7B7
A1U9-05	-DIFF CLOCK	3309780	7A5
A1U9-11	-DIFF CLOCK	3309780	7A4
A1U92-06*	+UPSPEED	3309780	8B6
A1U92-12	-SERVO SQUARE BITS (SQUARED SERVO BITS)	3309780	8B6
A1U93-01	-INDEX ENABLE	3309780	9B7
A1U93-04	-INDEX RESET	3309780	9B6
A1U93-08*	+INDEX	3309780	9B6
A1U94-10	-POWER FAIL (-PWR FAIL)	3309780	6B6
A1U95-04*	+SECTOR PULSE	3309780	9A4
A1U95-05	+9.67 CLOCK	3309780	11B1
A1U95-08*	+WRITE PROTECT	3309780	10B3
A1U95-09	-READ ONLY SW	3309780	10B2
A1U95-13	-9.67 CLOCK BUF 1	3309780	9C8
A1U97-01	-IP17	3309780	11C1
A1U97-02,05,06,09	I/O BUS	3309780	11C1
A1U97-03	+INDEX FOUND	3309780	11C1

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A1U97-04	+AM ACTIVE	3309780	11C1
A1U97-07	+SYNC FOUND	3309780	11C1
A1U97-11	+4 MHZ CLOCK	3309780	11C1
A1U97-12	I/O BUS	3309780	11C1
A1U97-13	+SYNC ERROR	3309780	11C1
A1U98-05*	+SYNC ERROR	3309780	11A4
A1U98-09*	+RD ERROR	3309780	11C2
A1U99-04	+INDEX FOUND	3309780	11A6
A1U99-06*	+WRITE	3309780	11A5
A251-01*	+R/W UNSAFE	3309760	2B5
A257-11	-HAR 1	3309760	4A4
A2J1-01	-WRITE DATA BUF	3309760	2D7
A2J1-03	-UNSAFE	3309760	1B8
A2J1-05	-READ DATA	3309760	3A1
A2J1-09	-AM ENABLE (-ADDRESS MARK ENABLE)	3309760	3B7
A2J1-13	-READ CLOCK	3309760	3A1
A2J1-14	-HD TAG (-HEAD TAG)	3309760	1B8
A2J1-15	-WRITE CLK (-WRITE CLOCK BUF)	3309760	2D7
A2J1-16	-GATED R/W UNSAFE (-R/W UNSAFE)	3309760	1B3
A2J1-17	-AM DETECTED	3309760	5C2
A2J1-19	-STROBE EARLY	3309760	3D8
A2J1-21	-STROBE LATE	3309760	3D8
A2J1-23	-WRITE GATE	3309760	1B8
A2J1-24	-GATED MULT HD (-MULTI CHIP SEL)	3309760	1B3
A2J1-25	-READ GATE	3309760	3B7
A2J1-26	-MODULE 8	3309760	1A8
A2J1-27	-OUTER TRACK	3309760	4A8
A2J1-28	-MODULE 4	3309760	1A8
A2J1-29	-MODULE 2	3309760	1A8
A2J1-30	-MODULE 1	3309760	1A8
A2J1-31	-HAR 4	3309760	2A8
A2J1-32	-HAR 8	3309760	2A8
A2J1-33	-HAR 1	3309760	4A8
A2J1-34	-HAR 2	3309760	4A8
A2J2-02	DY (DATA Y)	3309760	4C8
A2J2-03	DX (DATA X)	3309760	4C8
A2J2-05	-HS2 (-HEAD SELECT 2)	3309760	4B1
A2J2-07	WRITE CURRENT	3309760	4B1
A2J2-10	-HS1 (-HEAD SELECT 1)	3309760	4A1
A2J2-12	-CEMH 0 (CHIP EN 0)	3309760	2A1
A2J2-13	-MODULE 8	3309760	1A8
A2J2-14	-CEMH 1 (CHIP ENABLE 1)	3309760	2A1
A2J2-15	-MODULE 4	3309760	1A8
A2J2-16	-CEMH 2 (CHIP ENABLE 2)	3309760	2A1
A2J2-17	-MODULE 1	3309760	1A8
A2J2-18	-CEMH 3 (CHIP ENABLE 3)	3309760	2A1
A2J2-19	-MODULE 2	3309760	1A8
A2J2-20	WRITE SELECT (+WRITE SELECT)	3309760	4B1
A2J2-23	+6V R/W CHIP	3309760	2B1
A2J2-25	MARS UNSAFE	3309760	2A8
A2J3-01	+2FS (+2F)	3309760	2C7
A2J3-02	-2FS (-2F)	3309760	2C8
A2Q10B	DX (DATA X)	3309760	4C7
A2Q12B	+WRITE MFM	3309760	4C7
A2Q12C	DY (DATA Y)	3309760	4C8

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A2Q13B	-WRITE MFM	3309760	4C7
A2Q13C	DX (DATA X)	3309760	4C7
A2Q14E*	WRITE SELECT (+WRITE SELECT)	3309760	4B4
A2Q6B	-AM ENABLE (-ADDRESS MARK ENABLE)	3309760	4D2
A2Q6C*	THRESHOLD	3309760	4C2
A2Q9C*	WRITE CURRENT	3309760	4B6
A2U13-02	VFO TO (+VCO TO)	3309760	3C4
A2U16-11	2F PLO	3309760	2C5
A2U20-03*	VFO TO (+VCO TO)	3309760	3C4
A2U26-04	-RAW READ DATA	3309760	5A7
A2U26-05	+RAW READ DATA	3309760	5A7
A2U26-12	-2FS (-2F)	3309760	2C7
A2U26-13	+2FS (+2F)	3309760	2C7
A2U26-15*	2F PLO	3309760	2C7
A2U29-05	2 FPLO -(2 FPLO +2)	3309760	3C6
A2U29-06	+RAW READ DATA	3309760	3C7
A2U29-12	-READ GATE	3309760	3B7
A2U29-13	+HOLD	3309760	3B7
A2U30-06	-READ GATE	3309760	3B7
A2U31-03*	2 FPLO -(2 FPLO +2)	3309760	3C7
A2U31-06	2F PLO	3309760	3C7
A2U32-06	+AM WRITE	3309760	2C3
A2U34-08	+HOLD	3309760	5B2
A2U36-02	2F PLO	3309760	3C8
A2U36-03	2F PLO+2	3309760	5C7
A2U36-04	-RAW READ DATA	3309760	5A7
A2U36-07	+RAW READ DATA	3309760	5A8
A2U38-02*	+WRITE MFM	3309760	2B2
A2U38-03*	-WRITE MFM	3309760	2B2
A2U38-05	+RD GATE (+READ GATE)	3309760	2B2
A2U38-07	+AM WRITE	3309760	2C2
A2U39-01	-WRITE GATE	3309760	1B5
A2U39-05	-UNSAFE	3309760	1B5
A2U39-06*	-GATED WRITE	3309760	1B3
A2U39-11*	+UNSAFE	3309760	1B4
A2U39-12	-UNSAFE	3309760	1B5
A2U40-02	+MSC (+MCS)	3309760	1B5
A2U40-03	-HD TAG (-HEAD TAG)	3309760	1B7
A2U40-04	+R/W UNSAFE	3309760	1B5
A2U40-06	-UNSAFE	3309760	1C6
A2U41-06	+RAW READ DATA	3309760	3C7
A2U41-11	2 FPLO -(2 FPLO +2)	3309760	3C7
A2U43-01*	-READ GATE	3309760	3B7
A2U43-02*	-AM SEARCH	3309760	3B7
A2U43-03*	+READ GATE (+RD GATE)	3309760	3B7
A2U43-04*	+AM WRITE	3309760	3B7
A2U43-05	-AM ENABLE (-ADDRESS MARK ENABLE)	3309760	3B7
A2U43-07	-READ GATE	3309760	3B7
A2U43-10	-STROBE EARLY	3309760	3D8
A2U43-11	-STROBE LATE	3309760	3D8
A2U44-06	+RD GATE (+READ GATE)	3309760	2B7
A2U45-06	2F PLO+2	3309760	5C7
A2U46-02*	+HOLD	3309760	5B2
A2U47-03*	+DATA HOLD	3309760	5B7
A2U47-04	+VCO TO (VFO TO)	3309760	5B8

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A2U47-05	-READ GATE	3309760	5B7
A2U47-12	-READ GATE	3309760	5B7
A2U47-13	-AM SEARCH	3309760	5B7
A2U49-11	-AM ENABLE (-ADDRESS MARK ENABLE)	3309760	1B8
A2U5-04*	-AM DETECTED	3309760	5C2
A2U5-12*	-READ CLOCK	3309760	3A3
A2U5-13*	-READ DATA	3309760	3A3
A2U5-15	+DATA HOLD	3309760	3A3
A2U50-01	+MSC (+MCS)	3309760	1A5
A2U50-03*	-GATED MULT HD (-MULTI CHIP SEL)	3309760	1B3
A2U50-04	+R/W UNSAFE	3309760	1B4
A2U50-06*	-GATED R/W UNSAFE (-R/W UNSAFE)	3309760	1B3
A2U50-09	-UNSAFE	3309760	1B6
A2U50-12	-HD TAG (-HEAD TAG)	3309760	1B7
A2U50-13	-WRITE GATE	3309760	1B7
A2U51-06	MARS UNSAFE	3309760	2B6
A2U51-14*	+MCS (+MSC)	3309760	2A5
A2U52-09	ANALOG A	3309760	1D7
A2U52-10	ANALOG B	3309760	1D7
A2U53-10	THRESHOLD	3309760	1C7
A2U53-11	ANALOG B	3309760	1C7
A2U53-12	ANALOG A	3309760	1C7
A2U53-13	THRESHOLD	3309760	1C7
A2U56-10*	-RAW READ DATA	3309760	1C4
A2U56-11*	+RAW READ DATA	3309780	1C4
A2U57-10	-HAR 2	3309760	4B4
A2U59-01*	-CEMH 3 (CHIP ENABLE 3)	3309760	2A4
A2U59-02*	-CEMH 2 (CHIP ENABLE 2)	3309760	2A4
A2U59-03*	-CEMH 1 (CHIP ENABLE 1)	3309760	2A4
A2U59-04*	-CEMH 0 (CHIP EN 0)	3309760	2A4
A2U59-13	-UNSAFE	3309760	2A4
A2U59-14	HAR 8 (-HAR 8)	3309760	2A4
A2U59-15	HAR 4 (-HAR 4)	3309760	2A4
A2U6-02*	+GATED WS	3309760	1B3
A2U6-04*	-GATED WS	3309760	1B3
A2U6-05	-GATED WRITE	3309760	1B4
A2U6-07	-WRITE DATA	3309760	2D7
A2U6-10	-WRITE CLK (-WRITE CLOCK BUF)	3309760	2D7
A2U6-11	-GATED WRITE	3309760	2D7
A2U61-13*	-HS2 (-HEAD SELECT 2)	3309760	4B2
A2U62-08	-AM ENABLE (-ADDRESS MARK ENABLE)	3309760	4D3
A2U64-04	-OUTER TRACK	3309760	4A8
A2U64-10	-HAR 1	3309760	4A7
A2U65-09	-GATED WRITE	3309760	4B7
A2U65-10	-GATED WRITE	3309760	4B7
A2U66-02	-GATED WS	3309760	4B5
A2U66-04	+GATED WS	3309760	4B4
A2U66-07	WRITE CURRENT	3309760	4B5
A2U67-13*	-HS1 (-HEAD SELECT 1)	3309760	4A2
A2U69-07*	ANALOG A	3309760	4D4
A2U69-08*	ANALOG B	3309760	4D4
A2VR3*	+6V R/W CHIP	3309760	2B7
A348-11	+FEEDBACK PULSE TTL	3309770	2B8
A3C90	QP	3309770	5B8
A3CR26	AGC	3309770	1D8

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A3J1-01	+2F (+2 FS)	3309770	2C1
A3J1-02	-2F (-2 FS)	3309770	2C1
A3J2-02	CURRENT SENSE	3309770	7A3
A3J2-04*	MOTOR DRIVE	3309770	7C3
A3J3-01	-POWER ON RESET	3309770	3B8
A3J3-02*	SERVO VOLTAGE	3309770	7C3
A3J3-03	-SQUARED SERVO BITS(-SERVO SQUARE BITS)	3309770	1C2
A3J3-05	SERVO ONE BYTE TTL (+SERVO ONE BYTE)	3309770	3A4
A3J3-07	+PLO UNSAFE TTL (+PLO UNSAFE)	3309770	3B4
A3J3-08	-512 (-DIFF 512)	3309770	6C8
A3J3-09	-SERVO CLOCK TTL (+SERVO CLOCK)	3309770	3A3
A3J3-10	-M VEL (-MED VEL)	3309770	5B1
A3J3-11	-SERVO DISABLE	3309770	7C8
A3J3-12	CYL PULSE	3309770	5D1
A3J3-13	-2256 (-2 DIFF 256)	3309770	6C8
A3J3-14	-OFFSET	3309770	6C7
A3J3-15	-FINE TRACK	3309770	6B1
A3J3-16	-PLO	3309770	2B1
A3J3-17	+CAR 1	3309770	6B8
A3J3-19	+CAR 2	3309770	6B8
A3J3-20	-DIFF #0	3309770	6A8
A3J3-22	-LOCK ON	3309770	6A8
A3J3-23	-RUN	3309770	7C8
A3J3-24	-MOVE OUT	3309770	6C8
A3J3-25	-REZERO	3309770	5C8
A3J3-27	-128 (-DIFF 128)	3309770	6C8
A3J3-28	-64 (-DIFF 64)	3309770	6C8
A3J3-29	-8 (-DIFF 8)	3309770	6D8
A3J3-30	-32 (-DIFF 32)	3309770	6D8
A3J3-31	-4 (-DIFF 4)	3309770	6D8
A3J3-32	-16 (-DIFF 16)	3309770	6D8
A3J3-33	-2 (-DIFF 2)	3309770	6D8
A3J3-34	-1 (-DIFF 1)	3309770	6D8
A3J4-01	SERVO-Y (OUTPUT-)	3309770	1C8
A3J4-02	SERVO-X (OUTPUT+)	3309770	1C8
A3L10	SERVO-X (OUTPUT+)	3309770	1C8
A3L9	SERVO-Y (OUTPUT-)	3309770	1C8
A3Q6E*	+SERVO BITS	3309770	1C5
A3R120	QP	3309770	5C8
A3R121	QP	3309770	5D8
A3R137	ERROR AMPLIFIER	3309770	7C7
A3R138	CURRENT SENSE	3309770	7A6
A3R160	NP	3309770	5B7
A3R170	-GATE 1	3309770	4D8
A3R209	NP	3309770	5A7
A3R210	NP	3309770	5B7
A3R212	TACH-A	3309770	5B3
A3R219	-GATE 2	3309770	4D8
A3R227	-GATE 4	3309770	4B8
A3R23	SERVO VOLTAGE	3309770	7C3
A3R232	-GATE 3	3309770	4B8
A3R90	TACH A	3309770	6C4
A3R92	CURRENT SENSE	3309770	5A6
A3R93	NP	3309770	5D8
A3U1-01	-512 (-DIFF 512)	3309770	6C5

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A3U1-08	VEL COMP 1	3309770	6D4
A3U1-16	VEL COMP 2	3309770	6D5
A3U10-01*	+2F (+2 FS)	3309770	2C1
A3U10-02*	-2F (-2 FS)	3309770	2C1
A3U13-01	-1/2T	3309770	6D7
A3U13-02	-1 (-DIFF 1)	3309770	6D7
A3U13-03	-2 (-DIFF 2)	3309770	6D7
A3U13-04	-4 (-DIFF 4)	3309770	6D7
A3U13-05	-8 (-DIFF 8)	3309770	6D7
A3U13-16	-16 (-DIFF 16)	3309770	6D7
A3U13-17	-32 (-DIFF 32)	3309770	6D7
A3U13-18	-64 (-DIFF 64)	3309770	6C7
A3U13-19	-128 (-DIFF 128)	3309770	6C7
A3U18-05	-LOCK ON	3309770	6A4
A3U24-01	-OFFSET	3309770	6A7
A3U24-04	-2256 (-2 DIFF 256)	3309770	6C7
A3U24-11*	-1/2T	3309770	5D3
A3U24-13	-LOCK ON	3309770	5D3
A3U25-02*	-PLO	3309770	2B1
A3U25-04*	-FINE TRACK	3309770	6B3
A3U25-05	-DIFF #0	3309770	6A7
A3U25-08*	+MOVE OUT	3309770	5D5
A3U25-09	-MOVE OUT	3309770	5D6
A3U25-13	-LOCK ON	3309770	6A6
A3U27-05*	VELCOMP2	3309770	6A3
A3U27-08*	VELCOMP1	3309770	6A2
A3U27-10	+MOVE OUT	3309770	6A2
A3U27-12	-MOVE OUT	3309770	6A2
A3U3-01	-DIFF #0	3309770	6C3
A3U3-08,09	-MOVE OUT	3309770	6D4
A3U33-01,16	-SERVO DISABLE	3309770	7C7
A3U33-06	ERROR AMPLIFIER	3309770	7C7
A3U33-08	-RUN	3309770	7C7
A3U33-09	-REZERO	3309770	6C5
A3U34-01	-RUN	3309770	6A8
A3U34-02	+CAR 1	3309770	6A8
A3U34-03	+CAR 2	3309770	6A8
A3U34-14	CYL PULSE	3309770	5C5
A3U35-03	QP	3309770	6B7
A3U35-06	NP	3309770	6B7
A3U35-11	QP	3309770	6B7
A3U35-14	NP	3309770	6B7
A3U43-01	+MOVE OUT	3309770	5D5
A3U43-08*	CYL TRANS	3309770	5C6
A3U44-03	-M VEL (-MED VEL)	3309770	5A6
A3U44-03	-M VEL (-MED VEL)	3309770	5A6
A3U44-03	+SERVO CLOCK TTL (+SERVO CLOCK)	3309770	3A4
A3U44-05	-RUN	3309770	5C6
A3U44-08*	-SERVO CLOCK TTL (+SERVO CLOCK)	3309770	3A3
A3U44-10*	-SQUARED SERVO BITS(-SERVO SQUARE BITS)	3309770	1C2
A3U44-11	SQUARED SERVO BITS	3309770	1C2
A3U46-12	+P P XING	3309770	5A6
A3U46-13	+Q P XING	3309770	5A6
A3U47-05, 10	+QP	3309770	4D2
A3U47-07*	+QP XING	3309770	4B1

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A3U48-05	SQUARED SERVO BITS	3309770	2C8
A3U48-07	+PLO LOCKED TTL	3309770	2C8
A3U48-10	+SYNC GATE TTL	3309770	2B8
A3U5-01	-DIFF #0	3309770	6C4
A3U5-09	-OFFSET	3309770	6C5
A3U5-16,01	-LOCK ON	3309770	6B2
A3U50-01*	QP	3309770	4C2
A3U50-07*	NP	3309770	4B2
A3U52-01*	QP	3309770	4D3
A3U53-07*	NP	3309770	4A3
A3U54-05	-M VEL (-MED VEL)	3309770	4C8
A3U54-07	-H VEL	3309770	4C8
A3U54-09	NP	3309770	5C7
A3U55-07*, -12*	NP XING	3309770	4A1
A3U6-07*	ERROR AMP	3309770	6B2
A3U61-03,11	+SERVO CLOCK TTL (+SERVO CLOCK)	3309770	3B4
A3U61-05*	+PLO LOCKED TTL	3309770	3B4
A3U61-06*	+PLO UNSAFE TTL (+PLO UNSAFE)	3309770	3B4
A3U61-08*	+SERVO ONE BYTE	3309770	3A4
A3U61-12	+INDEX BYTE TTL	3309770	3A5
A3U62-05	+INDEX GATE TTL (+INDEX GATE)	3309770	2A8
A3U62-07	+SERVO CLOCK TTL	3309770	2A8
A3U64-07*	TACH-A	3309770	5C3
A3U65-08, -16	-M VEL (-MED VEL)	3309770	5B7
A3U65-09,01	-H VEL	3309770	5B8
A3U65-16,08	-M VEL (-MED VEL)	3309770	5B7
A3U66-01*,02*	-H VEL	3309770	5B2
A3U66-04	+INDEX BYTE TTL	3309770	3A7
A3U66-13*, -14*	-M VEL (-MED VEL)	3309770	5A2
A3U66-13*,14*	-M VEL (-MED VEL)	3309770	5B2
A3U68-03,06	+SERVO BITS	3309770	4A7
A3U70-03,11	+1F	3309770	3B4
A3U70-05*	+INDEX GATE (+INDEX GATE TTL)	3309770	3C4
A3U70-09*	+SYNC GATE TTL	3309770	3B4
A3U71-04*	+INDEX BYTE TTL	3309770	2A5
A3U71-05*	-SYNC BYTE TTL	3309770	2B6
A3U71-12*	+1F	3309770	2B1
A3U74-03,11	+1F	3309770	3C4
A3U75-01*	AGC	3309770	4C3
A3U76-04,13	+PLO LOCKED TTL	3309770	3C4
A3U77-14	+SERVO CLOCK TTL (+SERVO CLOCK)	3309770	3C5
A3U78-03,11	+1F	3309770	3D4
A3U78-10,01	+PLO LOCKED TTL	3309770	3D4
A3U79-02	+1F	3309770	3C6
A3U79-11*	+SERVO CLOCK TTL (+SERVO CLOCK)	3309770	3C6
A3U80-04*	SQUARED SERVO BITS	3309770	1C3
A3U81-01	+PLO UNSAFE TTL (+PLO UNSAFE)	3309770	2C5
A3U81-03	-REZERO	3309770	5C7
A3U81-06*	-GATE 1	3309770	3B3
A3U81-08*	-GATE 3	3309770	3C3
A3U81-10*	-GATE 4	3309770	3C3
A3U81-12*	-GATE 2	3309770	3C3
A3U82-03	+1F	3309770	3C7
A3U82-09*	+FEEDBACK PULSE TTL	3309770	3B4
A3U82-11	+1F	3309770	3B4

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A3U86-01	+PLO UNSAFE TTL (+PLO UNSAFE)	3309770	3A6
A3U86-13	-SYNC BYTE TTL	3309770	3A6
A3U87-01	-POWER ON RESET	3309770	3B6
A3U87-02	+SERVO CLOCK TTL (+SERVO CLOCK)	3309770	3B6
A3U87-09	-SYNC BYTE TTL	3309770	3B7
A3U89-01	-POWER ON RESET	3309770	3B6
A3U89-02	+SERVO CLOCK TTL (+SERVO CLOCK)	3309770	3B6
A4DS1-02	+D1SF	3310060	1D3
A4DS1-03	+D1SG	3310060	1D3
A4DS1-04	+D1SE	3310060	1D3
A4DS1-05	+D1SD	3310060	1D3
A4DS1-08	+D1SC	3310060	1D3
A4DS1-10	+D1SA	3310060	1D3
A4DS2-02	+D2SF	3310060	1D5
A4DS2-03	+D2SG	3310060	1D5
A4DS2-04	+D2SE	3310060	1D5
A4DS2-05	+D2SD	3310060	1D5
A4DS2-06	+D2SC	3310060	1D5
A4DS2-09	+D2SB	3310060	1D5
A4DS2-10	+D2SA	3310060	1D5
A4DS3-02	+D3SF	3310060	1D6
A4DS3-03	+D3SG	3310060	1D6
A4DS3-04	+D3SE	3310060	1D6
A4DS3-05	+D3SD	3310060	1D6
A4DS3-08	+D3SC	3310060	1D6
A4DS3-09	+D3SB	3310060	1D6
A4DS3-10	+D3SA	3310060	1D6
A4DS4-02	+D4SF	3310060	1D7
A4DS4-03	+D4SG	3310060	1D7
A4DS4-04	+D4SE	3310060	1D7
A4DS4-05	+D4SD	3310060	1D7
A4DS4-08	+D4SC	3310060	1D7
A4DS4-09	+D4SB	3310060	1D7
A4DS4-10	+D4SA	3310060	1D7
A4DS5-C	-SELECTED LED	3310060	1C7
A4DS6-C	-READY LED	3310060	1C7
A4DS7-C	-FAULT LED (-UNSAFE LED)	3310060	1B7
A4DS8-C	-READ ONLY LED (-RD ONLY LED)	3310060	1B7
A4J1-01	-COLUMN X2	3310060	1A7
A4J1-02	-COLUMN X1	3310060	1A8
A4J1-03	-COLUMN X4	3310060	1A7
A4J1-04	-COLUMN X3	3310060	1A8
A4J1-05	-ROW Y4	3310060	1A7
A4J1-06	-ROW Y3	3310060	1A7
A4J1-07	-ROW Y2	3310060	1B7
A4J1-08	-ROW Y1	3310060	1B7
A4J1-09	+D4SD	3310060	1D7
A4J1-10	+D4SE	3310060	1D7
A4J1-11	+D4SC	3310060	1D7
A4J1-12	+D4SB	3310060	1D7
A4J1-13	+D4SA	3310060	1D7
A4J1-14	+D4SG	3310060	1D7
A4J1-15	+D4SF	3310060	1D7
A4J1-16	+D2SB	3310060	1D5
A4J1-17	+D2SC	3310060	1D5

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A4J1-18	+D2SD	3310060	1D5
A4J1-19	+D2SE	3310060	1D5
A4J1-20	+D2SA	3310060	1D5
A4J1-21	+D2SG	3310060	1D5
A4J1-22	+D2SF	3310060	1D5
A4J1-23	+D1SF	3310060	1D4
A4J1-24	+D1SG	3310060	1D4
A4J1-25	+D1SA	3310060	1D4
A4J1-26	+D1SB	3310060	1D4
A4J1-27	+D1SC	3310060	1D4
A4J1-28	+D1SD	3310060	1D4
A4J1-29	+D1SE	3310060	1D4
A4J1-31	+D3SG	3310060	1D6
A4J1-32	+D3SA	3310060	1D6
A4J1-33	+D3SB	3310060	1D6
A4J1-34	+D3SC	3310060	1D6
A4J1-35	+D3SD	3310060	1D6
A4J1-36	+D3SF	3310060	1D6
A4J1-36	+D3SE	3310060	1D6
A4J1-37	-DIAGNOSTIC (DIAGNOSTICS SWITCH)	3310060	1B7
A4J1-39	-READ ONLY LED (-RD ONLY LED)	3310060	1C7
A4J1-40	-SELECTED LED (-SELECT LED)	3310060	1C7
A4J1-41	-READY LED	3310060	1C7
A4J1-42	-FAULT RESET SW	3310060	1B7
A4J1-43	-FAULT LED (-UNSAFE LED)	3310060	1B7
A4J1-44	-READ ONLY SW	3310060	1B7
A4KEYBD-01*	-COLUMN X1	3310060	1A7
A4KEYBD-02*	-COLUMN X2	3310060	1A7
A4KEYBD-03*	-COLUMN X3	3310060	1A6
A4KEYBD-04*	-COLUMN X4	3310060	1A6
A4KEYBD-05*	-ROW Y1	3310060	1A7
A4KEYBD-06*	-ROW Y2	3310060	1A7
A4KEYBD-07*	-ROW Y3	3310060	1A7
A4KEYBD-08*	-ROW Y4	3310060	1A7
A4S1*	-DIAGNOSTIC (DIAGNOSTICS SWITCH)	3310060	1B7
A4S2*	-FAULT RESET SW	3310060	1A7
A4S3*	-READ ONLY SW	3310060	1B7
A4SD-09	+D1SB	3310060	1D3
A5J1-01*, A5J2-01	BFT1-N	3316180	3C4
A5J1-02*, A5J2-02	BFT2-N	3316180	3C4
A5J1-03*, A5J2-03	BFT3-N	3316180	3B4
A5J1-04*, A5J2-04	BBS0-N	3316180	3D8
A5J1-05*, A5J2-05	BBS1-N	3316180	3D8
A5J1-06*, A5J2-06	BBS2-N	3316180	3C8
A5J1-07*, A5J2-07	BBS3-N	3316180	3C8
A5J1-08*, A5J2-08	BBS4-N	3316180	3B7
A5J1-09*, A5J2-09	BBS5-N	3316180	3B7
A5J1-10*, A5J2-10	BBS6-N	3316180	3B7
A5J1-11*, A5J2-11	BBS7-N	3316180	3A7
A5J1-12*, A5J2-12	BBS8-N	3316180	3D4
A5J1-13*, A5J2-13	BBS9-N	3316180	2B7
A5J1-14*, A5J2-14	BRDV-N	3316180	2C7
A5J1-15*	TBFT-N	3316180	4D5
A5J1-16*	TBSE-N	3316180	4C5
A5J1-17*, A5J2-17	TBCK-N	3316180	4C5

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A5J1-18*, A5J2-18	TBIN-N	3316180	4C5
A5J1-19*, A5J2-19	TBRD-N	3316180	4B5
A5J1-20*, A5J2-20	TBMK-N	3316180	4B5
A5J1-21*, A5J2-21	TBBY-N	3316180	4D2
A5J1-22*, A5J2-22	BRSL-N	3316180	2B7
A5J1-23*, A5J2-23	BRS0-N	3316180	2D7
A5J1-24*, A5J2-24	BRS1-N	3316180	2D7
A5J1-25*, A5J2-25	TBSC-N	3316180	4B5
A5J1-26*, A5J2-26	BRS2-N	3316180	2C7
A5J1-27*, A5J2-27	BRS3-N	3316180	2C7
A5J1-29*, A5J2-29	-BSQ1	3316180	2A7
A5J1-30*, A5J2-30	BB10-N	3316180	3C4
A5J1-31*, A5J2-31	BFT1-P	3316180	3C4
A5J1-32*, A5J2-32	BFT2-P	3316180	3C4
A5J1-33*, A5J2-33	BFT3-P	3316180	3B4
A5J1-34*, A5J2-34	BBS0-P	3316180	3D8
A5J1-35*, A5J2-35	BBS1-P	3316180	3C8
A5J1-36*, A5J2-36	BBS2-P	3316180	3C8
A5J1-37*, A5J2-37	BBS3-P	3316180	3C8
A5J1-38*, A5J2-38	BBS4-P	3316180	3B7
A5J1-39*, A5J2-39	BBS5-P	3316180	3B7
A5J1-40*, A5J2-40	BBS6-P	3316180	3B7
A5J1-41*, A5J2-41	BBS7-P	3316180	3A7
A5J1-42*, A5J2-42	BBS8-P	3316180	3C4
A5J1-43*, A5J2-43	BBS9-P	3316180	2B7
A5J1-44*, A5J2-44	BRDV-P	3316180	2C7
A5J1-45*, A5J2-45	TBFT-P	3316180	4D5
A5J1-46*, A5J2-46	TBSE-P	3316180	4C5
A5J1-47*, A5J2-47	TBCK-P	3316180	4C5
A5J1-48*, A5J2-48	TBIN-P	3316180	4C5
A5J1-49*, A5J2-49	TBRD-P	3316180	4B5
A5J1-51*, A5J2-51	TBBY-P	3316180	4D2
A5J1-52*, A5J2-52	BRSL-P	3316180	2B7
A5J1-53*, A5J2-53	BRS0-P	3316180	2D7
A5J1-54*, A5J2-54	BRS1-P	3316180	2D7
A5J1-55*, A5J2-55	TBSC-P	3316180	4B5
A5J1-56*, A5J2-56	BRS2-P	3316180	2C7
A5J1-57*, A5J2-57	BRS3-P	3316180	2C7
A5J1-58*, A5J2-58	TBWP-P	3316180	4A5
A5J1-59*, A5J2-59	BHL1	3316180	2A7
A5J1-60*, A5J2-60	BB10-P	3316180	3C4
A5J2-15	TBFT-N	3316180	4D5
A5J2-16	TBSE-N	3316180	4C5
A5J2-17	TBCK-N	3316180	4C5
A5J2-45	TBFT-P	3316180	4D5
A5J2-46	TBSE-P	3316180	4C5
A5J2-59	-BHL 0	3316180	4A5
A5J3-01	BSCK-G	3316180	4C2
A5J3-02	BSCK-P	3316180	4C1
A5J3-03	BRDT-P	3316180	4C1
A5J3-05	BRCK-P	3316180	4C1
A5J3-06*	BWCK-N	3316180	3A4
A5J3-07*	BWDT-G	3316180	3A4
A5J3-08*	BWDT-N	3316180	3A4
A5J3-09	BSEL-P	3316180	4B1

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A5J3-10	BSKN-N	3316 180	4B1
A5J3-12	BIDX-N	3316 180	4B1
A5J3-13	BSCT-N	3316 180	4B2
A5J3-14	BSCK-N	3316 180	4C1
A5J3-16	BRDT-N	3316 180	4C1
A5J3-16	BSCT-P	3316 180	4A2
A5J3-17	BRCK-N	3316 180	4C1
A5J3-18*	BWCK-G	3316 180	3A4
A5J3-19*	BWCK-P	3316 180	3A4
A5J3-20*	BWDI-P	3316 180	3A4
A5J3-22	BSEL-N	3316 180	4B1
A5J3-23	BSKN-P	3316 180	4B1
A5J3-24	BIDX-P	3316 180	4B1
A5J4-01	-BHL1	3316 180	1D7
A5J4-02	-BHLO	3316 180	1D7
A5J4-03	-BSQ1	3316 180	1D7
A5J4-04	-BSQ0	3316 180	1D7
A5J4-05	-READ DATA BUF 2	3316 180	1C7
A5J4-06	-READ CLOCK BUF 2	3316 180	1C7
A5J4-07	-9.67 CLOC BUF 2	3316 180	1C7
A5J4-08	-WRITE CLOCK	3316 180	1D7
A5J4-09	-WRITE DATA	3316 180	1C7
A5J4-10	-A CONTROL TAG	3316 180	1C7
A5J4-11	-B BUS 8	3316 180	1C7
A5J4-12	-B BUS 10	3316 180	1C7
A5J4-13	-CYLINDER TAG	3316 180	1C7
A5J4-14	-HEAD TAG (-HD TAG)	3316 180	1C7
A5J4-15	-B BUS 1	3316 180	1C7
A5J4-16	-B BUS 0	3316 180	1C7
A5J4-17	-B BUS 2	3316 180	1C7
A5J4-18	-B BUS 3	3316 180	1C7
A5J4-19	-B BUS 5	3316 180	1C7
A5J4-20	-B BUS 4	3316 180	1C7
A5J4-21	-B BUS 6	3316 180	1C7
A5J4-22	-B BUS 7	3316 180	1C7
A5J4-23	-A BUS 9	3316 180	1C7
A5J4-24	-B RELEASE	3316 180	1C7
A5J4-25	-A RELEASE	3316 180	1C7
A5J4-26	+A RESERVED	3316 180	1C7
A5J4-27	-B SELECTED	3316 180	1B7
A5J4-28	-A SELECTED	3316 180	1C7
A5J4-29	-B BUS 9	3316 180	1B7
A5J4-30	-DIAGNOSTICS	3316 180	1C7
A5J4-31	-B RESERVED	3316 180	1B7
A5J4-32	-4 MHZ CLOCK	3316 180	1C7
A5J4-33	-A RAW SELECT	3316 180	1C7
A5J4-34	-A INHIBIT	3316 180	1B7
A5J4-35	+UNSAFE	3316 180	1C7
A5J4-36	+SEEK INCOMPLETE	3316 180	1C7
A5J4-37	+INDEX	3316 180	1C7
A5J4-38	+ON CYLINDER	3316 180	1C7
A5J4-39	+FILE READY	3316 180	1B7
A5J4-40	-AM DETECTED	3316 180	1B7
A5J4-42	-B CONTROL TAG	3316 180	1B7
A5J4-43	+WRITE PROTECT	3316 180	1B7

**ASSY/
COMPONENT/PIN**
TERM
**SCHEM.
DIAGRAM**
**SHEET
COORD.**

A5J4-44	+SECTOR PULSE	3316180	1B7
A5J4-47	-SELECT SW1	3316180	1B7
A5J4-48	-SELECT SW0	3316180	1B7
A5J4-49	-SELECT SW3	3316180	1B7
A5J4-50	-SELECT SW2	3316180	1B7
A5J4-59	-POWER ON RESET	3316180	1A7
A5RN10-01	BFT1-P	3316180	3C4
A5RN10-03	BFT1-N	3316180	3C4
A5RN10-06	BB10-P	3316180	3C4
A5RN10-07	BB10-N	3316180	3C4
A5RN11-01	BFT2-P	3316180	3C4
A5RN11-03	BFT2-N	3316180	3C4
A5RN11-05	BBS8-P	3316180	3D4
A5RN11-07	BBS8-N	3316180	3D4
A5RN12-01	BFT3-N	3316180	3B4
A5RN12-03	BFT3-P	3316180	3B4
A5RN14-01	BWDT-G	3316180	3A4
A5RN14-01	BWCK-G	3316180	3A4
A5RN14-02	BWDT-P	3316180	3A4
A5RN14-03	BWDT-N	3316180	3A4
A5RN14-05	BWCK-N	3316180	3A4
A5RN14-07	BWCK-P	3316180	3A4
A5RN2-01	BRS1-N	3316180	2D6
A5RN2-03	BRS1-P	3316180	2D6
A5RN2-05	BRS0-N	3316180	2D6
A5RN2-07	BRS0-P	3316180	2D6
A5RN3-01	BRS3-N	3316180	2C6
A5RN3-03	BRS3-P	3316180	2C6
A5RN3-05	BRS2-N	3316180	2C6
A5RN3-07	BRS2-P	3316180	2C6
A5RN4-01	BBS0-N	3316180	3D7
A5RN4-03	BBS0-P	3316180	3D7
A5RN4-05	BBS1-N	3316180	3D7
A5RN4-07	BBS1-P	3316180	3D7
A5RN5-01	BBS3-N	3316180	3C7
A5RN5-03	BBS3-P	3316180	3C7
A5RN5-05	BBS2-N	3316180	3C7
A5RN5-07	BBS2-P	3316180	3C7
A5RN6-01	BBS5-N	3316180	3B7
A5RN6-03	BBS5-P	3316180	3B7
A5RN6-05	BBS4-N	3316180	3B7
A5RN6-07	BBS4-P	3316180	3B7
A5RN7-01	BBS7-N	3316180	3A7
A5RN7-03	BBS7-P	3316180	3A7
A5RN7-05	BBS6-N	3316180	3A7
A5RN7-07	BBS6-P	3316180	3A7
A5RN8-01	BBS9-P	3316180	2B6
A5RN8-03	BBS9-N	3316180	2B6
A5RN8-05	BRDV-N	3316180	2C6
A5RN8-07	BRDV-P	3316180	2C6
A5RN9-01	BRSL-P	3316180	2B6
A5RN9-03	BRSL-N	3316180	2B6
A5U10-01	+A RESERVED	3316180	5C7
A5U10-05	-A RAW SELECT	3316180	5D6
A5U10-08*	-B RESERVED	3316180	5B7

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A5U10-09	+B RESERVED	3316180	5B6
A5U10-11	+B RESERVED	3316180	5B2
A5U10-13	+A RESERVED	3316180	5C2
A5U11-05*	+B SELECTED	3316180	5B5
A5U11-06*	-B SELECTED	3316180	5B4
A5U12-01	+A RESERVED	3316180	5A7
A5U12-02	-A RAW SELECT	3316180	5A7
A5U12-05	-B SELECTED	3316180	5B4
A5U12-10	-A SELECTED	3316180	5D4
A5U12-12	+B RESERVED	3316180	5A7
A5U12-13	-B RAW SELECT	3316180	5A7
A5U13-03*	-B BUS 3	3316180	3C6
A5U13-04	-B PORT ENABLE	3316180	3C6
A5U13-05*	-B BUS 2	3316180	3C6
A5U13-11*	-B BUS 1	3316180	3C6
A5U13-13*	-B BUS 0	3316180	3D6
A5U14-03*	-B BUS 7	3316180	3A6
A5U14-04	-B PORT ENABLE	3316180	3A6
A5U14-05*	-B BUS 6	3316180	3B6
A5U14-11*	-B BUS 4	3316180	3B6
A5U14-13*	-B BUS 5	3316180	3B6
A5U15-03*	+OPEN CABLE DETECT	3316180	2B5
A5U15-13*	-B BUS 9	3316180	2B4
A5U16-03*	-B SELECT 3	3316180	2C4
A5U16-04	+OPEN CABLE DETECT	3316180	2C5
A5U16-05*	-B SELECT 2	3316180	2C4
A5U16-11*	-B SELECT 1	3316180	2D4
A5U16-13*	-B SELECT 0	3316180	2D4
A5U17-01	SELECT SW3	3316180	5B7
A5U17-09	-SELECT SW0	3316180	5B7
A5U17-10	-B SELECT 0	3316180	5C7
A5U17-11	SELECT SW1	3316180	5B7
A5U17-12	-B SELECT 1	3316180	5C7
A5U17-13	-B SELECT 2	3316180	5C7
A5U17-14	SELECT SW2	3316180	5B7
A5U17-15	-B SELECT 3	3316180	5C7
A5U18-02	-POWER ON RESET	3316180	5B7
A5U18-04	-DIAGNOSTICS	3316180	5D2
A5U18-06*	-DISABLE B	3316180	5D2
A5U18-13	+B SELECTED	3316180	5A4
A5U19-05*	+A RESERVED	3316180	5C2
A5U19-07*	+B RESERVED	3316180	5C2
A5U2-09	-A RAW SELECT	3316180	5C6
A5U2-13	-B RAW SELECT	3316180	5B6
A5U21-06*	-B PRIORITY	3316180	5C4
A5U21-08*	-A PRIORITY	3316180	5D4
A5U22-03	+B SELECTED	3316180	5B5
A5U23-01	-A RELEASE	3316180	5C7
A5U23-02	-A CONTROL TAG	3316180	5C7
A5U23-04	-B CONTROL TAG	3316180	5B7
A5U23-05	-B RELEASE	3316180	5B7
A5U23-11*	-B SELECT ENABLE	3316180	2B4
A5U23-13	+OPEN CABLE DETECT	3316180	2B4
A5U24-02*	+B PORT ENABLE	3316180	5B2
A5U24-03	-A SELECTED	3316180	5D5

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A5U24-05	-4 MHZ CLOCK	3316180	5B7
A5U24-09	-DISABLE B	3316180	2A5
A5U24-11	-B SELECT ENABLE	3316180	5B7
A5U24-12*	+B BUS 9	3316180	2B4
A5U25-01*	-A INHIBIT	3316180	5B2
A5U25-05	+A RESERVED	3316180	5A3
A5U25-06	+ON CYLINDER	3316180	5A2
A5U25-16*	+B SEEK END	3316180	5A2
A5U26-01	-A PRIORITY	3316180	5A6
A5U26-04	-POWER ON RESET	3316180	5B6
A5U26-10	-POWER ON RESET	3316180	5C6
A5U26-13	-B PRIORITY	3316180	5A6
A5U27-02	-B RAW SELECT	3316180	5B5
A5U27-05	-A RAW SELECT	3316180	5C5
A5U27-09	+OPEN CABLE DETECT	3316180	5B7
A5U27-13	-A BUS 9	3316180	5D7
A5U29-03*	-B BUS 8	3316180	3C2
A5U29-04	-B PORT ENABLE	3316180	3C2
A5U29-05*	-HEAD TAG (-HD TAG)	3316180	3C2
A5U29-11*	-CYLINDER TAG	3316180	3C2
A5U29-13*	-B BUS 10	3316180	3C2
A5U30-03*	-WRITE CLOCK	3316180	3A2
A5U30-04	-B PORT ENABLE	3316180	3A2
A5U30-05*	-WRITE DATA	3316180	3A2
A5U30-13*	-B CONTROL TAG	3316180	3B2
A5U31-01	+A RESERVED	3316180	4D3
A5U31-03	+B SELECTED	3316180	4C3
A5U31-06	-9.67 CLOCK BUF 2	3316180	4C3
A5U31-08*	BSCK-P	3316180	4C2
A5U31-09*	BSCK-N	3316180	4C2
A5U31-10, A5U32-10	-DISABLE B	3316180	4C3
A5U31-12*	TBBY-N	3316180	4D3
A5U31-13*	TBBY-P	3316180	4D3
A5U32-01	-READ DATA BUF 2	3316180	4C3
A5U32-05	-READ CLOCK BUF 2	3316180	4C3
A5U32-08*	BRCK-P	3316180	4C2
A5U32-09*	BRCK-N	3316180	4C2
A5U32-12*	BRDT-N	3316180	4C2
A5U32-13*	BRDT-P	3316180	4C2
A5U32-15	+B SELECTED	3316180	4B3
A5U33-01	+SECTOR PULSE	3316180	4B3
A5U33-02*	BSCT-P	3316180	4A3
A5U33-03*	BSCT-N	3316180	4B3
A5U33-04*	BIDX-N	3316180	4B2
A5U33-05*	BIDX-P	3316180	4B2
A5U33-06	-DISABLE B	3316180	4A3
A5U33-07	+INDEX	3316180	4B3
A5U33-10	+B SEEK END	3316180	4B3
A5U33-11*	BSKN-P	3316180	4B2
A5U33-12*	BSKN-N	3316180	4B2
A5U33-13*	BSEL-N	3316180	4B2
A5U33-14*	BSEL-P	3316180	4B2
A5U4-02	+A RESERVED	3316180	5D3
A5U4-11	-4 MHZ CLOCK	3316180	5B3
A5U4-12	+B RESERVED	3316180	5B3

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A5U5-01	+INDEX	3316180	4C7
A5U5-02*	TBIN-P	3316180	4C6
A5U5-03*	TBIN-N	3316180	4C6
A5U5-04*	TBCK-P	3316180	4C6
A5U5-05*	TBCK-N	3316180	4C7
A5U5-06	+B PORT ENABLE	3316180	4A7
A5U5-07	+ON CYLINDER	3316180	4C7
A5U5-10	+UNSAFE	3316180	4D7
A5U5-11*	TBFT-P	3316180	4D7
A5U5-12*	TBFT-N	3316180	4D7
A5U5-13*	TBSE-N	3316180	4C7
A5U5-14*	TBSE-P	3316180	4C7
A5U5-15	+SEEK INCOMPLETE	3316180	4D7
A5U6-01	+SECTOR PULSE	3316180	4B7
A5U6-02*	TBSO-P	3316180	4B6
A5U6-03*	TBSO-N	3316180	4B6
A5U6-04*	TBWP-N	3316180	4A6
A5U6-05*	TBWP-P	3316180	4A5
A5U6-07	+WRITE PROTECT	3316180	4A7
A5U6-10	-AM DETECTED	3316180	4B7
A5U6-11*	TBMK-N	3316180	4B6
A5U6-13*	TBRD-N	3316180	4B6
A5U6-14*	TBRD-P	3316180	4B6
A5U6-15	+FILE READY	3316180	4B7
A5U7-02	+A RESERVED	3316180	5A4
A5U7-08*	-B RAW SELECT	3316180	5B6
A5U8-05	-B SELECT ENABLE	3316180	5B7
A5U8-08*	-B PORT ENABLE	3316180	5B3
A5U8-09	+B RESERVED	3316180	5B2
A5U8-10	-DIAGNOSTICS	3316180	5B3
A6DS1-A	+RELAY DRIVE	3309790	3B4
A6DS2-A	+RELAY DRIVE	3309790	3B4
A6DS3-A	+RELAY DRIVE	3309790	3B4
A6DS4-A	+RELAY DRIVE	3309790	3A4
A6J2-01	+BRAKE COIL	3309790	3C3
A6J2-02	-BRAKE RETN	3309790	3C3
A6J2-03	-RUN RELAY DRIVE	3309790	3B3
A6J2-04	-START RELAY DRIVE	3309790	3B3
A6J2-05	+RELAY DRIVE	3309790	3B4
A6J3-01	MOTOR HI	3309790	3D3
A6J3-02	MOTOR LO	3309790	3D3
A6J4-09	-RUN	3309790	3D7
A6J4-11	-PWR FAIL (-POWER FAIL)	3309790	3A4
A6J5-02*	MTR I FDBK	3309790	3D3
A6J5-04	MOTOR DRIVE	3309790	3D8
A6K1-04*	MOTOR HI	3309790	3D3
A6K1-05	MOTOR DRIVE	3309790	3D5
A6Q15-C*	+BRAKE COIL	3309790	3C6
A6U10-06	-RUN	3309790	3C7
A6U11-01	-RUN	3309790	3B7
A6U11-03*	-RUN RELAY DRIVE	3309790	3B7
A6U11-05*	-START RELAY DRIVE	3309790	3B7
A6U7-08*	-PWR FAIL (-POWER FAIL)	3309790	3A4
A6U8-06	-RUN	3309790	3D6
A7J1-02	DATA Y (DY)	3309800	1D3

ASSY/ COMPONENT/PIN	TERM	SCHEM. DIAGRAM	SHEET COORD.
A7J1-03	DATA X (DX)	3309800	1D3
A7J1-05	-HEAD SELECT 2 (-HS2)	3309800	1D3
A7J1-07	WRITE CURRENT	3309800	1D3
A7J1-10	-HEAD SELECT 1 (-HS1)	3309800	1C3
A7J1-12	-CHIP EN 0 (CEMH 0)	3309800	1C3
A7J1-13	MODULE 8	3309800	1C3
A7J1-14	-CHIP ENABLE 1 (CEMH 1)	3309800	1C3
A7J1-15	MODULE 4	3309800	1C3
A7J1-16	-CHIP ENABLE 2 (CEMH 2)	3309800	1C3
A7J1-17	-MODULE 1	3309800	1C3
A7J1-18	-CHIP ENABLE 3 (CEMH 3)	3309800	1C3
A7J1-19	MODULE 2	3309800	1C3
A7J1-20	+WRITE SELECT (+WRITE SELECT)	3309800	1C3
A7J1-25*	MARS UNSAFE	3309800	1B3
A7J1-27*	OUTPUT -(SERVO-Y)	3309800	1B2
A7J1-28*	OUTPUT +(SERVO-X)	3309800	1B2
A7J1-29,30,33,34	SERVO GROUND	3309800	1B3
A7JUMPER-01*	-MODULE 1	3309800	1A5
A7JUMPER-02*	-MODULE 2	3309800	1A5
A7JUMPER-04*	-MODULE 4	3309800	1A5
A7JUMPER-08*	-MODULE 8	3309800	1A5
U1J2-29	-BSQ 1	3309780	4A1

LOGIC TERM SOURCES

This section includes an alpha-numeric list of all source logic terms for the Capricorn disk drive. The intent of this list is to assist the user in locating the source of logic signals. Moreover, this list is intended for reference use only and is not intended to be used as a wire list. In some cases, identical terms are given different term names. In these cases, the alternate term name is also listed in parenthesis. See Figure 3.

NOTE

The origin(s) of each signal is denoted by an asterisk (*).

Capricorn assembly designations are as follows:

- A1 -- I/O Control PCBA (CTROL)
- A2 -- Read/Write PCBA (READW)
- A3 -- Servo Driver PCBA (SERDV)
- A4 -- Diagnostic Control PCBA (DICO2)
- A5 -- Dual Port PCBA (DUPOC)
- A6 -- Power Supply Regulator PCBA (REGUL)
- A7 -- HDA Interface PCBA (HDAIN)

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
- OPEN CABLE DETECT	AlU59-12*	3309780	1B5
+ OPEN CABLE DETECT	A5U15-03*	3316180	2B5
- OUTER TRACK	AlU42-12*	3309780	7C4
OUTPUT +(SERVO-X)	A7J1-28*	3309800	1B2
OUTPUT -(SERVO-Y)	A7J1-27*	3309800	1B2
+ OUTWARD	AlU82-14*	3309780	10B5
- PLO	A3U25-02*	3309770	2B1
+ PLO LOCKED TTL	A3U61-05*	3309770	3B4
+ PLO UNSAFE TTL (+PLO UNSAFE)	A3U61-06*	3309770	3B4

SYMBOL INDICATES POLARITY OF SIGNAL WHEN ASSERTED (ABSENCE OF SIGN INDICATES POSITIVE POLARITY)	ALPHA-NUMERIC TERM	IDENTICAL SIGNAL WITH ALTERNATE TERM NAME (SEE ALTERNATE TERM NAME FOR REMAINING SIGNAL DESTINATION(S) OR ORIGIN(S).	PCBA	COMPONENT	PIN	INDICATES SIGNAL ORIGIN	SCHEMATIC DRAWING NO.	COORDINATES	SHEET NO. OF DRAWING
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Figure 3

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-1/2T	A3U24-11*	3309770	5D3
+1F	A3U71-12*	3309770	2B1
2 FPLO -(2 FPLO +2)	A2U31-03*	3309760	3C7
+2F (+2 FS)	A3U10-01*	3309770	2C1
-2F (-2 FS)	A3U10-02*	3309770	2C1
2F PLO	A2U26-15*	3309760	2C7
-4 MHZ CLOCK	A1U16-04*	3309780	4C4
+4 MHZ CLOCK	A1U35-02*	3309780	6C7
+6V R/W CHIP	A2VR3*	3309760	2B7
+9.67 CLOCK	A1U74-08*	3309780	11C7
-9.67 CLOCK BUF 1	A1U40-03*	3309780	3D5
-9.67 CLOCK BUF 2 (-9.67 CLK)	A1U40-18*	3309780	3D4
-A BUS 9	A1U6-11*	3309780	1A5
-A CONTROL TAG	A1U11-13*	3309780	1D2
-A INHIBIT	A5U25-01*	3316180	5B2
+A OR B SELECTED	A1U15-03*	3309780	4C3
+A PORT ENABLE	A1U18-12*	3309780	4D3
-A PORT ENABLE	A1U37-03*	3309780	4D3
-A PRIORITY	A5U21-08*	3316180	5D4
-A RAW SELECT	A1U26-06*	3309780	4C5
-A RELEASE	A1U15-06*	3309780	4B4
+A RESERVED	A5U19-05*	3316180	5C2
-A SELECT 0	A1U2-11*	3309780	1D5
-A SELECT 1	A1U2-13*	3309780	1C5
-A SELECT 2	A1U2-05*	3309780	1C5
-A SELECT 3	A1U2-03*	3309780	1C5
-A SELECT ENABLE	A1U35-12*	3309780	1B5
-A SELECTED	A1U26-08*	3309780	4C3
+A SELECTED	A1U26-09*	3309780	4C3
ABS0-N	A1J1-04*	3309780	2D8
ABS0-P	A1J1-34*	3309780	2D8
ABS1-N	A1J1-05*	3309780	2D8
ABS1-P	A1J1-35*	3309780	2D8
ABS10-N	A1J1-30*	3309780	2D4
ABS10-P	A1J1-60*	3309780	2D4
ABS2-N	A1J1-06*	3309780	2C8
ABS2-P	A1J1-36*	3309780	2C8
ABS3-N	A1J1-07*	3309780	2C8
ABS3-P	A1J1-37*	3309780	2C8
ABS4-N	A1J1-08*	3309780	2B8
ABS4-P	A1J1-38*	3309780	2B8
ABS5-N	A1J1-09*	3309780	2B8
ABS5-P	A1J1-39*	3309780	2B8
ABS6-N	A1J1-10*	3309780	2B8
ABS6-P	A1J1-40*	3309780	2B8
ABS7-N	A1J1-11*	3309780	2B8
ABS7-P	A1J1-41*	3309780	2A8
ABS8-N	A1J1-12*	3309780	2D4
ABS8-P	A1J1-42*	3309780	2D4
ABS9-N	A1J1-13*	3309780	1A8
ABS9-P	A1J1-43*	3309780	1A8
-ADDRESS MARK ENABLE (-AM ENABLE)	A1U33-11*	3309780	5B6
AFT1-N	A1J1-01*	3309780	2C4
AFT1-P	A1J1-31*	3309780	2C4
AFT2-N	A1J1-02*	3309780	2C4
AFT2-P	A1J1-32*	3309780	2C4

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
AFT3-N	A1J1-03*	3309780	2B4
AFT3-P	A1J1-33*	3309780	2B4
AGC	A3U75-01*	3309770	4C3
-AHL 1	A1J1-59*	3309780	4A8
AIDX-N	A1U12-03*	3309780	3B2
AIDX-P	A1U12-02*	3309780	3A2
+AM ACTIVE	A1U106-05*	3309780	11B3
-AM DETECTED	A2U5-04*	3309760	5C2
-AM SEARCH	A2U43-02*	3309760	3B7
+AM WRITE	A2U43-04*	3309760	3B7
ANALOG A	A2U69-07*	3309760	4D4
ANALOG B	A2U69-08*	3309760	4D4
ARCK-N	A1U21-13*	3309780	3C2
ARCK-P	A1U21-12*	3309780	3C2
ARDT-N	A1U21-08*	3309780	3C3
ARDT-P	A1U21-09*	3309780	3C2
ARDV-N	A1J1-14*	3309780	1C8
ARDV-P	A1J1-44*	3309780	1B8
ARSO-N	A1J1-23*	3309780	1D8
ARSO-P	A1J1-53*	3309780	1D8
ARS1-N	A1J1-24*	3309780	1D8
ARS1-P	A1J1-54*	3309780	1C8
ARS2-N	A1J1-26*	3309780	1C8
ARS2-P	A1J1-56*	3309780	1C8
ARS3-N	A1J1-27*	3309780	1C8
ARS3-P	A1J1-57*	3309780	1C8
ARSL-N	A1J1-22*	3309780	1B8
ARSL-P	A1J1-52*	3309780	1A8
ASCK-N	A1U20-08*	3309780	3C2
ASCK-P	A1U20-09*	3309780	3C2
ASCT-N	A1U12-04*	3309780	3A2
ASCT-P	A1U12-05*	3309780	3A2
ASEL-N	A1U12-12*	3309780	3B2
ASEL-P	A1U12-11*	3309780	3B2
ASKN-N	A1U12-13*	3309780	3B2
ASKN-P	A1U12-14*	3309780	3B2
-ASQ 1	A1J1-29*	3309780	4A8
AWCK-N	A1J3-06*	3309780	2A4
AWCK-P	A1J3-19*	3309780	2A4
AWDT-N	A1J3-08*	3309780	2B4
AWDT-P	A1J3-20*	3309780	2B4
-B BUS 0	A5U13-13*	3316180	3D6
-B BUS 1	A5U13-11*	3316180	3C6
-B BUS 10	A1U3-11*	3309780	2D2
-B BUS 10	A5U29-13*	3316180	3C2
-B BUS 2	A5U13-05*	3316180	3C6
-B BUS 3	A5U13-03*	3316180	3C6
-B BUS 4	A5U14-11*	3316180	3B6
-B BUS 5	A5U14-13*	3316180	3B6
-B BUS 6	A5U14-05*	3316180	3B6
-B BUS 7	A5U14-03*	3316180	3A6
-B BUS 8	A1U3-13*	3309780	2D2
-B BUS 8	A5U29-03*	3316180	3C2
-B BUS 9	A5U15-13*	3316180	2B4
+B BUS 9	A5U24-12*	3316180	2B4
-B CONTROL TAG	A5U30-13*	3316180	3B2

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
+B PORT ENABLE	A5U24-02*	3316180	5B2
-B PORT ENABLE	A5U8-08*	3316180	5B3
-B PRIORITY	A5U21-06*	3316180	5C4
-B RAW SELECT	A5U7-08*	3316180	5B6
-B RESERVED	A5U10-08*	3316180	5B7
+B RESERVED	A5U19-07*	3316180	5C2
+B SEEK END	A5U25-16*	3316180	5A2
-B SELECT 0	A5U16-13*	3316180	2D4
-B SELECT 1	A5U16-11*	3316180	2D4
-B SELECT 2	A5U16-05*	3316180	2C4
-B SELECT 3	A5U16-03*	3316180	2C4
-B SELECT ENABLE	A5U23-11*	3316180	2B4
+B SELECTED	A5U11-05*	3316180	5B5
-B SELECTED	A5U11-06*	3316180	5B4
BB10-N	A5J1-30*, A5J2-30	3316180	3C4
BB10-P	A5J1-60*, A5J2-60	3316180	3C4
BBS0-N	A5J1-04*, A5J2-04	3316180	3D8
BBS0-P	A5J1-34*, A5J2-34	3316180	3D8
BBS1-N	A5J1-05*, A5J2-05	3316180	3D8
BBS1-P	A5J1-35*, A5J2-35	3316180	3C8
BBS2-N	A5J1-06*, A5J2-06	3316180	3C8
BBS2-P	A5J1-36*, A5J2-36	3316180	3C8
BBS3-N	A5J1-07*, A5J2-07	3316180	3C8
BBS3-P	A5J1-37*, A5J2-37	3316180	3C8
BBS4-N	A5J1-08*, A5J2-08	3316180	3B7
BBS4-P	A5J1-38*, A5J2-38	3316180	3B7
BBS5-N	A5J1-09*, A5J2-09	3316180	3B7
BBS5-P	A5J1-39*, A5J2-39	3316180	3B7
BBS6-N	A5J1-10*, A5J2-10	3316180	3B7
BBS6-P	A5J1-40*, A5J2-40	3316180	3B7
BBS7-N	A5J1-11*, A5J2-11	3316180	3A7
BBS7-P	A5J1-41*, A5J2-41	3316180	3A7
BBS8-N	A5J1-12*, A5J2-12	3316180	3D4
BBS8-P	A5J1-42*, A5J2-42	3316180	3C4
BBS9-N	A5J1-13*, A5J2-13	3316180	2B7
BBS9-P	A5J1-43*, A5J2-43	3316180	2B7
BFT1-N	A5J1-01*, A5J2-01	3316180	3C4
BFT1-P	A5J1-31*, A5J2-31	3316180	3C4
BFT2-N	A5J1-02*, A5J2-02	3316180	3C4
BFT2-P	A5J1-32*, A5J2-32	3316180	3C4
BFT3-N	A5J1-03*, A5J2-03	3316180	3B4
BFT3-P	A5J1-33*, A5J2-33	3316180	3B4
BHL1	A5J1-59*, A5J2-59	3316180	2A7
BIDX-N	A5U33-04*	3316180	4B2
BIDX-P	A5U33-05*	3316180	4B2
+BRAKE COIL	A6Q15-C*	3309790	3C6
BRCK-N	A5U32-09*	3316180	4C2
BRCK-P	A5U32-08*	3316180	4C2
BRDT-N	A5U32-12*	3316180	4C2
BRDT-P	A5U32-13*	3316180	4C2
BRDV-N	A5J1-14*, A5J2-14	3316180	2C7
BRDV-P	A5J1-44*, A5J2-44	3316180	2C7
BRS0-N	A5J1-23*, A5J2-23	3316180	2D7
BRS0-P	A5J1-53*, A5J2-53	3316180	2D7
BRS1-N	A5J1-24*, A5J2-24	3316180	2D7
BRS1-P	A5J1-54*, A5J2-54	3316180	2D7

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
BRS2-N	A5J1-26*, A5J2-26	3316180	2C7
BRS2-P	A5J1-56*, A5J2-56	3316180	2C7
BRS3-N	A5J1-27*, A5J2-27	3316180	2C7
BRS3-P	A5J1-57*, A5J2-57	3316180	2C7
BRSL-N	A5J1-22*, A5J2-22	3316180	2B7
BRSL-P	A5J1-52*, A5J2-52	3316180	2B7
BSCK-N	A5U31-09*	3316180	4C2
BSCK-P	A5U31-08*	3316180	4C2
BSCT-N	A5U33-03*	3316180	4B3
BSCT-P	A5U33-02*	3316180	4A3
BSEL-N	A5U33-13*	3316180	4B2
BSEL-P	A5U33-14*	3316180	4B2
BSKN-N	A5U33-12*	3316180	4B2
BSKN-P	A5U33-11*	3316180	4B2
-BSQ1	A5J1-29*, A5J2-29	3316180	2A7
-BUS 0	A1RP-02*	3309780	2D5
+BUS 0	A1U14-12*	3309780	5C7
-BUS 1	A1RP-08*	3309780	2D5
+BUS 1	A1U14-04*	3309780	5C7
-BUS 10	A1RP1-04*	3309780	2D2
-BUS 2	A1RP-03*	3309780	2C5
+BUS 2	A1U14-02*	3309780	5B7
-BUS 3	A1RP-04*	3309780	2C5
+BUS 3	A1U13-02*	3309780	5B7
-BUS 4	A1RP-06*	3309780	2B4
+BUS 4	A1U13-06*	3309780	5B7
-BUS 5	A1RP-05*	3309780	2B4
+BUS 5	A1U14-08*	3309780	5B7
-BUS 6	A1RP-07*	3309780	2B6
BUS 6	A1U13-10*	3309780	5C5
-BUS 7	A1RP-08*	3309780	2A6
+BUS 7	A1U13-08*	3309780	5B7
+BUS 8	A1U14-10*	3309780	5A7
+BUS 9	A1U15-11*	3309780	4B4
BWCK-G	A5J3-18*	3316180	3A4
BWCK-N	A5J3-06*	3316180	3A4
BWCK-P	A5J3-19*	3316180	3A4
BWDT-G	A5J3-07*	3316180	3A4
BWDT-N	A5J3-08*	3316180	3A4
BWDT-P	A5J3-20*	3316180	3A4
+CAR 1	A1U42-02*	3309780	7C4
+CAR 2	A1U42-05*	3309780	7C4
-CEMH 0 (CHIP EN 0)	A2U59-04*	3309760	2A4
-CEMH 1 (CHIP ENABLE 1)	A2U59-03*	3309760	2A4
-CEMH 2 (CHIP ENABLE 2)	A2U59-02*	3309760	2A4
-CEMH 3 (CHIP ENABLE 3)	A2U59-01*	3309760	2A4
-COLUMN X1	A1U120-11*	3309780	10A6
-COLUMN X1	A4KEYBD-01*	3310060	1A7
-COLUMN X2	A1U120-10*	3309780	10A6
-COLUMN X2	A4KEYBD-02*	3310060	1A7
-COLUMN X3	A1U120-08*	3309780	10A6
-COLUMN X3	A4KEYBD-03*	3310060	1A6
-COLUMN X4	A1U120-07*	3309780	10A6
-COLUMN X4	A4KEYBD-04*	3310060	1A6
-CONTROLLER RESET	A1U33-06*	3309780	5B6
CYL PULSE	A3U43-08*	3309770	5C6

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-CYLINDER TAG	A1U3-03*	3309780	2C2
-CYLINDER TAG	A5U29-11*	3316180	3C2
-D BUS 0	A1U22-03*	3309780	11A5
-D BUS 0	A1U24-11*	3309780	11D2
-D BUS 1	A1U23-12*	3309780	11A5
-D BUS 1	A1U24-03*	3309780	11D2
-D BUS 2	A1U24-06*	3309780	11D2
-D BUS 3	A1U24-08*	3309780	11D2
-D BUS 5	A1U23-08*	3309780	11B2
-D CONTROL TAG	A1U100-06*	3309780	11A6
+D1SA	A1U123-13*	3309780	10A2
+D1SB	A1U123-12*	3309780	10A2
+D1SC	A1U123-11*	3309780	10A2
+D1SD	A1U123-10*	3309780	10A2
+D1SE	A1U123-09*	3309780	10A2
+D1SF	A1U123-15*	3309780	10A2
+D1SG	A1U123-14*	3309780	10A2
+D2SA	A1U122-13*	3309780	10A3
+D2SB	A1U122-12*	3309780	10A3
+D2SC	A1U122-11*	3309780	10A3
+D2SD	A1U122-10*	3309780	10A3
+D2SE	A1U122-09*	3309780	10A3
+D2SF	A1U122-15*	3309780	10A3
+D2SG	A1U122-14*	3309780	10A3
+D3SA	A1U124-13*	3309780	10A4
+D3SB	A1U124-12*	3309780	10A4
+D3SC	A1U124-11*	3309780	10A4
+D3SD	A1U124-10*	3309780	10A4
+D3SE	A1U124-09*	3309780	10A4
+D3SF	A1U124-15*	3309780	10A4
+D3SG	A1U124-14*	3309780	10A4
+D4SA	A1U121-13*	3309780	10A5
+D4SB	A1U121-12*	3309780	10A5
+D4SC	A1U121-11*	3309780	10A5
+D4SD	A1U121-10*	3309780	10A5
+D4SE	A1U121-09*	3309780	10A5
+D4SF	A1U121-15*	3309780	10A5
+D4SG	A1U121-14*	3309780	10A5
+DATA AVAILABLE	A1U120-12*	3309780	10B6
+DATA HOLD	A2U14-14*	3309760	3A5
+DATA HOLD	A2U47-03*	3309760	5B7
+DHAR 1	A1U46-02*	3309780	11D7
+DHAR 2	A1U46-05*	3309780	11D7
+DHAR 4	A1U46-06*	3309780	11D7
+DHAR 8	A1U46-09*	3309780	11D7
-DIAGNOSTIC (DIAGNOSTICS SWITCH)	A4S1*	3310060	1B7
-DIAGNOSTICS	A1U17-08*	3309780	4C6
-DIAGNOSTICS TEST	A1U43-02*	3309780	7B3
-DIFF 1 (-1)	A1U19-03*	3309780	7C2
-DIFF 1024 (-1024)	A1U30-06*	3309780	7D2
-DIFF 128 (-128)	A1U31-07*	3309780	7C2
-DIFF 16 (-16)	A1U31-03*	3309780	7C2
-DIFF 2 (-2)	A1U19-02*	3309780	7B2
-DIFF 256 (-256)	A1U30-03*	3309780	7D2
-2DIFF 256 (-2256)	A1U30-12*	3309780	7D2
-DIFF 32 (-32)	A1U31-02*	3309780	7C2

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-DIFF 4 (-4)	A1U19-06*	3309780	7B2
-DIFF 512 (-512)	A1U30-02*	3309780	7D2
-DIFF 64 (-64)	A1U3-06*	3309780	7C2
-DIFF 8 (-8)	A1U19-07*	3309780	7B2
+DIFF #0	A1U68-08*	3309780	7C2
-DIFF #0	A1U69-08*	3309780	7D2
-DIFF CLOCK	A1U25-10*	3309780	8B3
-DISABLE A	A1U16-13*	3309780	1A7
-DISABLE A	A1U17-11*	3309780	4B6
-DISABLE B	A5U18-06*	3316180	5D2
+EN SEQ TNU	A1U42-15*	3309780	7C4
-ERROR 4	A1U84-06*	3309780	10D6
ERROR AMP	A3U6-07*	3309770	6B2
-FAULT RESET SW	A4S2*	3310060	1A7
+FEEDBACK PULSE TTL	A3U82-09*	3309770	3B4
+FILE READY	A1U17-03*	3309780	10D1
-FINE TRACK	A3U25-04*	3309770	6B3
-GATE 1	A3U81-06*	3309770	3B3
-GATE 2	A3U81-12*	3309770	3C3
-GATE 3	A3U81-08*	3309770	3C3
-GATE 4	A3U81-10*	3309770	3C3
-GATED MULT HD (-MULTI CHIP SEL)	A2U50-03*	3309760	1B3
-GATED R/W UNSAFE (-R/W UNSAFE)	A2U50-06*	3309760	1B3
-GATED WRITE	A2U39-06*	3309760	1B3
+GATED WS	A2U6-02*	3309760	1B3
-GATED WS	A2U6-04*	3309760	1B3
+GB ERROR	A1U76-09*	3309780	8C3
-H VEL	A3U66-01*,02*	3309770	5B2
-HAR 1	A1U63-04*	3309780	5C5
-HAR 2	A1U63-07*	3309780	5C5
-HAR 4	A1U63-09*	3309780	5C5
-HAR 8	A1U63-12*	3309780	5C5
-HEAD TAG (-HD TAG)	A1U22-06*	3309780	11C2
-HEAD TAG (-HD TAG)	A1U3-05*	3309780	2C2
-HEAD TAG (-HD TAG)	A5U29-05*	3316180	3C2
+HOLD	A2U46-02*	3309760	5B2
-HS1 (-HEAD SELECT 1)	A2U67-13*	3309760	4A2
-HS2 (-HEAD SELECT 2)	A2U61-13*	3309760	4B2
I/O BUS	A1U119-02*	3309780	7C5
I/O BUS	A1U119-05*	3309780	7C5
I/O BUS	A1U119-06*	3309780	7C5
I/O BUS	A1U119-09*	3309780	7C5
I/O BUS	A1U119-12*	3309780	7C5
I/O BUS	A1U119-15*	3309780	7C5
I/O BUS	A1U119-16*	3309780	7C5
I/O BUS	A1U119-19*	3309780	7C5
I/O BUS	A1U19-01*	3309780	7C3
I/O BUS	A1U19-09*	3309780	7C3
I/O BUS	A1U19-10*	3309780	7C3
I/O BUS	A1U19-15*	3309780	7C3
I/O BUS	A1U30-01*	3309780	7D3
I/O BUS	A1U30-09*	3309780	7D3
I/O BUS	A1U30-10*	3309780	7D3
I/O BUS	A1U30-15*	3309780	7D3
I/O BUS	A1U31-01*	3309780	7C3
I/O BUS	A1U31-09*	3309780	7C3

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
I/O BUS	A1U31-10*	3309780	7C3
I/O BUS	A1U31-15*	3309780	7C3
I/O BUS	A1U41-03*	3309780	7D4
I/O BUS	A1U41-04*	3309780	7D4
I/O BUS	A1U41-07*	3309780	7D4
I/O BUS	A1U41-08*	3309780	7D4
I/O BUS	A1U41-13*	3309780	7D4
I/O BUS	A1U41-14*	3309780	7D4
I/O BUS	A1U41-17*	3309780	7D4
I/O BUS	A1U41-18*	3309780	7D4
I/O BUS	A1U42-03*	3309780	7C4
I/O BUS	A1U42-04*	3309780	7C4
I/O BUS	A1U42-07*	3309780	7C4
I/O BUS	A1U42-08*	3309780	7C4
I/O BUS	A1U42-13*	3309780	7C4
I/O BUS	A1U42-14*	3309780	7C4
I/O BUS	A1U42-17*	3309780	7C4
I/O BUS	A1U42-18*	3309780	7C4
I/O BUS	A1U43-03*	3309780	7C4
I/O BUS	A1U43-04*	3309780	7C4
I/O BUS	A1U43-07*	3309780	7C4
I/O BUS	A1U43-08*	3309780	7C4
I/O BUS	A1U43-13*	3309780	7C4
I/O BUS	A1U43-14*	3309780	7C4
I/O BUS	A1U43-17*	3309780	7C4
I/O BUS	A1U43-18*	3309780	7C4
I/O BUS	A1U44-02*	3309780	7C7
I/O BUS	A1U44-05*	3309780	7C7
I/O BUS	A1U44-06*	3309780	7C7
I/O BUS	A1U44-09*	3309780	7C7
I/O BUS	A1U44-12*	3309780	7C7
I/O BUS	A1U44-15*	3309780	7C7
I/O BUS	A1U44-16*	3309780	7C7
I/O BUS	A1U44-19*	3309780	7C7
I/O BUS	A1U45-02*	3309780	7D7
I/O BUS	A1U45-05*	3309780	7D7
I/O BUS	A1U45-06*	3309780	7D7
I/O BUS	A1U45-09*	3309780	7D7
I/O BUS	A1U45-12*	3309780	7D7
I/O BUS	A1U45-15*	3309780	7D7
I/O BUS	A1U45-16*	3309780	7D7
I/O BUS	A1U45-19*	3309780	7D7
I/O BUS	A1U64-02*	3309780	7C5
I/O BUS	A1U64-05*	3309780	7C5
I/O BUS	A1U64-06*	3309780	7C5
I/O BUS	A1U64-09*	3309780	7C5
I/O BUS	A1U64-12*	3309780	7C5
I/O BUS	A1U64-15*	3309780	7C5
I/O BUS	A1U64-16*	3309780	7C5
I/O BUS	A1U64-19*	3309780	7C5
I/O BUS	A1U65-11* THRU 18*	3309780	6B3
I/O BUS	A1U85-02*	3309780	7C7
I/O BUS	A1U85-05*	3309780	7C7
I/O BUS	A1U85-06*	3309780	7C7
I/O BUS	A1U85-09*	3309780	7C7
I/O BUS	A1U85-12*	3309780	7C7

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
I/O BUS	A1U85-15*	3309780	7C7
I/O BUS	A1U85-16*	3309780	7C7
I/O BUS	A1U85-19*	3309780	7C7
I/O BUS	A1U86-02*	3309780	7D5
I/O BUS	A1U86-05*	3309780	7D5
I/O BUS	A1U86-06*	3309780	7D5
I/O BUS	A1U86-09*	3309780	7D5
I/O BUS	A1U86-12*	3309780	7D5
I/O BUS	A1U86-15*	3309780	7D5
I/O BUS	A1U86-16*	3309780	7D5
I/O BUS	A1U86-19*	3309780	7D5
I/O BUS	A1U87-02*	3309780	7B7
I/O BUS	A1U87-05*	3309780	7B7
I/O BUS	A1U87-06*	3309780	7B7
I/O BUS	A1U87-09*	3309780	7B7
I/O BUS	A1U87-12*	3309780	7B7
I/O BUS	A1U87-15*	3309780	7B7
I/O BUS	A1U87-16*	3309780	7B7
I/O BUS	A1U87-19*	3309780	7B7
+INDEX	A1U93-08*	3309780	9B6
+INDEX BYTE TTL	A3U71-04*	3309770	2A5
-INDEX ENABLE	A1U53-10*	3309780	8C6
+INDEX FOUND	A1U100-05*	3309780	11A6
+INDEX GATE (+INDEX GATE TTL)	A3U70-05*	3309770	3C4
-INDEX RESET	A1U52-06*	3309780	8C7
-INITIALIZE	A1U73-12*	3309780	6A2
-INTERRUPT	A1U51-08*	3309780	5B3
+INWARD	A1U82-13*	3309780	10C5
-IP10	A1U72-15*	3309780	6D2
-IP11	A1U72-14*	3309780	6D2
-IP12	A1U72-13*	3309780	6D2
-IP13	A1U72-12*	3309780	6D2
-IP14	A1U72-11*	3309780	6C2
-IP15	A1U72-10*	3309780	6C2
-IP16	A1U72-09*	3309780	6C2
-IP17	A1U72-07*	3309780	6C2
+KEY 1	A1U120-17*	3309780	10B6
+KEY 2	A1U120-16*	3309780	10B6
+KEY 4	A1U120-15*	3309780	10B6
+KEY 8	A1U120-14*	3309780	10B6
-LOCK ON	A1U41-09*	3309780	7D4
-M VEL (-MED VEL)	A3U66-13*, -14*	3309770	5A2
-M VEL (-MED VEL)	A3U66-13*, 14*	3309770	5B2
MARS UNSAFE	A7J1-25*	3309800	1B3
+MCS (+MSC)	A2U51-14*	3309760	2A5
-MODULE 1	A7JUMPER-01*	3309800	1A5
-MODULE 2	A7JUMPER-02*	3309800	1A5
-MODULE 4	A7JUMPER-04*	3309800	1A5
-MODULE 8	A7JUMPER-08*	3309800	1A5
MOTOR DRIVE	A3J2-04*	3309770	7C3
MOTOR HI	A6K-04*	3309790	3D3
-MOVE OUT	A1U41-05*	3309780	7D4
+MOVE OUT	A3U25-08*	3309770	5D5
MTR I FDBK	A6J5-02*	3309790	3D3
NP	A3U50-07*	3309770	4B2
NP	A3U53-07*	3309770	4A3

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
NP XING	A3U55-07*, -12*	3309770	4A1
+ODD HEAD	A1U42-06*	3309780	7C4
-OFFSET	A1U41-06*	3309780	7D4
+OFFSET FORWARD	A1U36-08*	3309780	5B6
+OFFSET REVERSE	A1U36-11*	3309780	5B6
-OFFSET SELECT	A1U34-01*	3309780	5B5
+OGB #1	A1U60-10*	3309780	8C3
OGB #2	A1U60-06*	3309780	8B3
+ON CYLINDER	A1U36-03*	3309780	5B3
+ON TRACK	A1U41-12*	3309780	7D4
-OP20	A1U70-15*	3309780	6C2
-OP21	A1U70-14*	3309780	6C2
-OP22	A1U70-13*	3309780	6C2
-OP23	A1U70-12*	3309780	6C2
-OP24	A1U70-11*	3309780	6C2
-OP25	A1U122-03*	3309780	10A3
-OP25	A1U123-03*	3309780	10A3
-OP25	A1U70-10*	3309780	6C2
-OP26	A1U70-09*	3309780	6C2
-OP40	A1U73-15*	3309780	6B2
-OP41	A1U73-14*	3309780	6B2
-OP42	A1U73-13*	3309780	6B2
-OP43	A1U71-12*	3309780	6B2
-OP44	A1U73-11*	3309780	6B2
-OP45	A1U73-10*	3309780	6B2
-OPEN CABLE DETECT	A1U59-12*	3309780	1B5
+OPEN CABLE DETECT	A5U15-03*	3316180	2B5
-OUTER TRACK	A1U42-12*	3309780	7C4
OUTPUT +(SERVO-X)	A7J1-28*	3309800	1B2
OUTPUT -(SERVO-Y)	A7J1-27*	3309800	1B2
+OUTWARD	A1U82-14*	3309780	10B5
-PLO	A3U25-02*	3309770	2B1
+PLO LOCKED TTL	A3U61-05*	3309770	3B4
+PLO UNSAFE TTL (+PLO UNSAFE)	A3U61-06*	3309770	3B4
POWER ON RESET	A1U114-10*	3309780	6A6
-PWR FAIL (-POWER FAIL)	A6U7-08*	3309790	3A4
QP	A3U50-01*	3309770	4C2
QP	A3U52-01*	3309770	4D3
+QP XING	A3U47-07*	3309770	4B1
+R/W UNSAFE	A251-01*	3309760	2B5
-RAW READ DATA	A2U56-10*	3309760	1C4
+RAW READ DATA	A2U56-11*	3309780	1C4
+RD ERROR	A1U98-09*	3309780	11C2
-RD ONLY LED (-READ ONLY LED)	A1U114-12*	3309780	10B1
+READ	A1U100-09*	3309780	11A4
-READ CLOCK	A2U5-12*	3309760	3A3
-READ CLOCK BUF 1	A1U40-12*	3309780	3B4
-READ CLOCK BUF 2 (-CLOCK)	A1U40-09*	3309780	3B4
-READ DATA	A2U5-13*	3309760	3A3
-READ DATA BUF 1	A1U40-14*	3309780	3B4
-READ DATA BUF 2 (-DATA)	A1U40-07*	3309780	3C4
-READ GATE	A1U37-08*	3309780	5C6
-READ GATE	A2U43-01*	3309760	3B7
+READ GATE (+RD GATE)	A2U43-03*	3309760	3B7
-READ ONLY SW	A4S3*	3310060	1B7
+READY	A1U41-15*	3309780	7C4

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-READY LED	A1U114-06*	3309780	10C1
-RESET	A1U112-11*	3309780	11B5
-RESET GB ERROR	A1U71-11*	3309780	6A2
-RESET INTERRUPT	A1U71-13*	3309780	6A2
-RESET UNSAFE	A1U71-14*	3309780	6B2
-REZERO	A1U59-10*	3309780	7C3
+REZERO INT	A1U39-06*	3309780	5C4
-ROW Y1	A4KEYBD-05*	3310060	1A7
-ROW Y2	A4KEYBD-06*	3310060	1A7
-ROW Y3	A4KEYBD-07*	3310060	1A7
-ROW Y4	A4KEYBD-08*	3310060	1A7
+RUN	A1U42-19*	3309780	7C4
-RUN	A1U69-12*	3309780	7C4
-RUN RELAY DRIVE	A6U11-03*	3309790	3B7
+SECTOR PULSE	A1U95-04*	3309780	9A4
+SEEK INCOMPLETE	A1U41-19*	3309780	7C4
+SEEK INT	A1U39-08*	3309780	5A4
-SELECT LED (-SELECTED LED)	A1U114-02*	3309780	10B1
-SELECT SW0	A1S4-01*	3309780	4C7
-SELECT SW1	A1S4-02*	3309780	4C7
-SELECT SW2	A1S4-03*	3309780	4C7
-SELECT SW3	A1S4-04*	3309780	4C7
-SEQUENCE HOLD	A1U29-12*, A1U29-07	3309780	4B6
-SEQUENCE PICK	A1U29-02*, A1U29-14	3309780	4A6
-SERVO BITS	A3Q6E*	3309770	1C5
-SERVO CLOCK TTL (+SERVO CLOCK)	A3U44-08*	3309770	3A3
+SERVO CLOCK TTL (+SERVO CLOCK)	A3U79-11*	3309770	3C6
-SERVO DISABLE	A1U41-16*	3309780	7C4
SERVO ONE BYTE TTL (+SERVO ONE BYTE)	A3U61-08*	3309770	3A4
SERVO VOLTAGE	A3J3-02*	3309770	7C3
-SET UNSAFE	A1U71-15*	3309780	6B2
+SPLIT FIELD	A1U42-09*	3309780	7C4
SQUARED SERVO BITS	A3U80-04*	3309770	1C3
-SQUARED SERVO BITS(-SERVO SQUARE BITS)	A3U44-10*	3309770	1C2
-START	A1U69-10*	3309780	7C3
-START RELAY DRIVE	A6U11-05*	3309790	3B7
-STROBE EARLY	A1U33-08*	3309780	5B6
-STROBE LATE	A1U33-03*	3309780	5A6
-SYNC BYTE TTL	A3U71-05*	3309770	2B6
+SYNC ERROR	A1U98-05*	3309780	11A4
+SYNC FOUND	A1U108-05*	3309780	11A4
+SYNC GATE TTL	A3U70-09*	3309770	3B4
TABY-N	A1U20-12*	3309780	3D2
TABY-P	A1U20-13*	3309780	3D2
TACH-A	A3U64-07*	3309770	5C3
TACY-N	A1U7-04*	3309780	3C7
TACY-P	A1U7-05*	3309780	3C7
TAFT-N	A1U7-12*	3309780	3D7
TAFT-P	A1U7-11*	3309780	3D7
TAIN-N	A1U7-03*	3309780	3C7
TAIN-P	A1U7-02*	3309780	3C7
TAMK-N	A1U8-14*	3309780	3B7
TAMK-P	A1U8-13*	3309780	3B7
TARD-N	A1U8-12*	3309780	3B7
TARD-P	A1U8-11*	3309780	3B7
TASC-N	A1U8-04*	3309780	3B7

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
TASC-P	A1U8-05*	3309780	3A7
TASE-N	A1U7-13*	3309780	3D7
TASE-P	A1U7-14*	3309780	3D7
TAWP-N	A1U8-03*	3309780	3A7
TAWP-P	A1U8-02*	3309780	3A7
TBBY-N	A5J1-21*, A5J2-21	3316180	4D2
TBBY-N	A5U31-12*	3316180	4D3
TBBY-P	A5J1-51*, A5J2-51	3316180	4D2
TBBY-P	A5U31-13*	3316180	4D3
TBCK-N	A5J1-17*, A5J2-17	3316180	4C5
TBCK-N	A5U5-05*	3316180	4C7
TBCK-P	A5J1-47*, A5J2-47	3316180	4C5
TBCK-P	A5U5-04*	3316180	4C6
TBFT-N	A5J1-15*	3316180	4D5
TBFT-N	A5U5-12*	3316180	4D7
TBFT-P	A5J1-45*, A5J2-45	3316180	4D5
TBFT-P	A5U5-11*	3316180	4D7
TBIN-N	A5J1-18*, A5J2-18	3316180	4C5
TBIN-N	A5U5-03*	3316180	4C6
TBIN-P	A5J1-48*, A5J2-48	3316180	4C5
TBIN-P	A5U5-02*	3316180	4C6
TBMK-N	A5J1-20*, A5J2-20	3316180	4B5
TBMK-N	A5U6-11*	3316180	4B6
TBRD-N	A5J1-19*, A5J2-19	3316180	4B5
TBRD-N	A5U6-13*	3316180	4B6
TBRD-P	A5J1-49*, A5J2-49	3316180	4B5
TBRD-P	A5U6-14*	3316180	4B6
TBSC-N	A5J1-25*, A5J2-25	3316180	4B5
TBSC-P	A5J1-55*, A5J2-55	3316180	4B5
TBSE-N	A5J1-16*	3316180	4C5
TBSE-N	A5U5-13*	3316180	4C7
TBSE-P	A5J1-46*, A5J2-46	3316180	4C5
TBSE-P	A5U5-14*	3316180	4C7
TBSO-N	A5U6-03*	3316180	4B6
TBSO-P	A5U6-02*	3316180	4B6
TBWP-N	A5U6-04*	3316180	4A6
TBWP-P	A5J1-58*, A5J2-58	3316180	4A5
TBWP-P	A5U6-05*	3316180	4A5
THRESHOLD	A2Q6C*	3309760	4C2
-UNSAFE	A1U35-08*	3309780	10D3
+UNSAFE	A1U76-04*	3309780	10C3
+UNSAFE	A2U39-11*	3309760	1B4
+UNSAFE CLOCK	A1U112-03*	3309780	10C1
-UNSAFE LED (-FAULT LED)	A1U114-04*	3309780	10C1
+UPSPEED	A1U92-06*	3309780	8B6
VELCOMP1	A3U27-08*	3309770	6A2
VELCOMP2	A3U27-05*	3309770	6A3
VFO TO (+VCO TO)	A2U20-03*	3309760	3C4
+WRITE	A1U99-06*	3309780	11A5
-WRITE CLOCK	A1U11-05*	3309780	2A2
-WRITE CLOCK	A1U22-08*	3309780	11A6
-WRITE CLOCK	A5U30-03*	3316180	3A2
-WRITE CLOCK BUF (-WRITE CLK)	A1U40-05*	3309780	3C4
WRITE CURRENT	A2Q9C*	3309760	4B6
-WRITE DATA	A1U11-03*	3309780	2B2
-WRITE DATA	A1U22-11*	3309780	11C2

TERM	ASSY/ COMPONENT/PIN	SCHEM. DIAGRAM	SHEET COORD.
-WRITE DATA	A5U30-05*	3316180	3A2
-WRITE DATA BUF	A1U40-16*	3309780	3C4
-WRITE ERROR	A1U84-14*	3309780	10C6
-WRITE GATE	A1U37-06*	3309780	5C6
+WRITE MFM	A2U38-02*	3309760	2B2
-WRITE MFM	A2U38-03*	3309760	2B2
+WRITE PATTERN	A1U108-09*	3309780	11B4
+WRITE PROTECT	A1U95-08*	3309780	10B3
WRITE SELECT (+WRITE SELECT)	A2Q14E*	3309760	4B4